INVESTOR DAY PRESENTATION

June 12, 2025

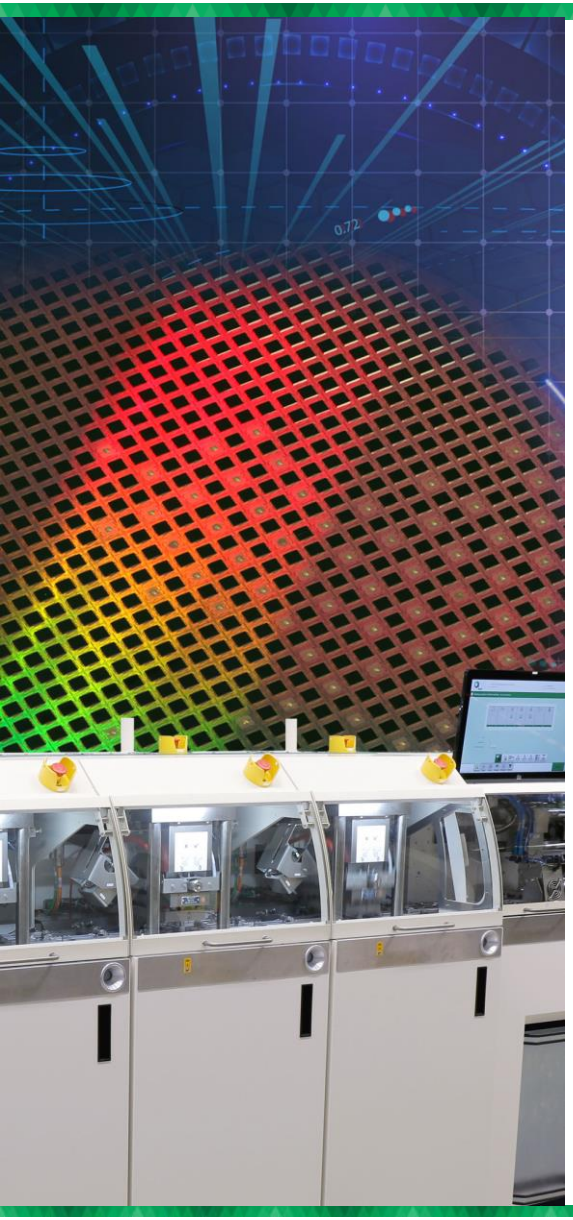
Safe Harbor Statement

This presentation contains statements about management's future expectations, plans and prospects of our business that constitute forward-looking statements, which are found in various places throughout the presentation, including, but not limited to, statements relating to expectations of orders, net sales, product shipments, expenses, timing of purchases of assembly equipment by customers, gross margins, operating results and capital expenditures. The use of words such as “anticipate”, “estimate”, “expect”, “can”, “intend”, “believes”, “may”, “plan”, “predict”, “project”, “forecast”, “will”, “would”, and similar expressions are intended to identify forward-looking statements, although not all forward-looking statements contain these identifying words. The financial guidance set forth under the heading “Outlook” contains such forward-looking statements. While these forward-looking statements represent our judgments and expectations concerning the development of our business, a number of risks, uncertainties and other important factors could cause actual developments and results to differ materially from those contained in forward-looking statements, including any inability to maintain continued demand for our products; failure of anticipated orders to materialize or postponement or cancellation of orders, generally without charges; the volatility in the demand for semiconductors and our products and services; the extent and duration of the COVID-19 and other global pandemics and the associated adverse impacts on the global economy, financial markets, global supply chains and our operations as well as those of our customers and suppliers; failure to develop new and enhanced products and introduce them at competitive price levels; failure to adequately decrease costs and expenses as revenues decline; loss of significant customers, including through industry consolidation or the emergence of industry alliances; lengthening of the sales cycle; acts of terrorism and violence; disruption or failure of our information technology systems; consolidation activity and industry alliances in the semiconductor industry that may result in further increased customer concentration, inability to forecast demand and inventory levels for our products; the integrity of product pricing and protection of our intellectual property in foreign jurisdictions; risks, such as changes in trade regulations, conflict minerals regulations, currency fluctuations, political instability and war, associated with substantial foreign customers, suppliers and foreign manufacturing operations, particularly to the extent occurring in the Asia Pacific region where we have a substantial portion of our production facilities; potential instability in foreign capital markets; the risk of failure to successfully manage our diverse operations; any inability to attract and retain skilled personnel, including as a result of restrictions on immigration, travel or the availability of visas for skilled technology workers.

In addition, the United States and other countries have recently levied tariffs and taxes on certain goods and could significantly increase or impose new tariffs on a broad array of goods. They have imposed, and may continue to impose, new trade restrictions and export regulations. Increased or new tariffs and additional taxes, including any retaliatory measures, trade restrictions and export regulations, could negatively impact end-user demand and customer investment in semiconductor equipment, increase Besi’s supply chain complexity and manufacturing costs, decrease margins, reduce the competitiveness of our products or restrict our ability to sell products, provide services or purchase necessary equipment and supplies. Any or all of the foregoing factor could have a material and adverse effect on our business, results of operations or financial condition. In addition, investors should consider those additional risk factors set forth in Besi's annual report for the year ended December 31, 2024 and other key factors that could adversely affect our businesses and financial performance contained in our filings and reports, including our statutory consolidated statements. We expressly disclaim any obligation to update or alter our forward-looking statements whether as a result of new information, future events or otherwise.

Agenda

I.	Strategic Overview	Richard Blickman	13.00 – 13.20
II.	Market Trends	Chris Scanlan	13.20 – 13.50
III.	Wafer Level Assembly	Peter Wiedner	13.50 – 14.15
	Break		14.15 – 14.30
IV.	Mainstream Die Attach	Christoph Scheiring	14.30 – 14.45
V.	Strategic Plan Update	Richard Blickman	14.45 – 15.00
VI.	Q&A	Besi Team	15.00



I. STRATEGIC OVERVIEW
Richard Blickman
CEO

Besi's Opportunity

AI Expansion Drives Continued Advanced Packaging Adoption

- Generative AI accelerating. Large capex budgets maintained by hyperscalers
- New use cases emerging from cloud to edge computing
- Accelerated advanced packaging innovation expected in 2026-2030 across logic, memory, consumer & I/O
- Advanced packaging one of key differentiators to realize AI promise including energy efficient performance in data centers and new consumer edge AI devices

Assembly at Major Growth Inflection Point

- Promise of AI requires new 2.5D/3D assembly solutions to further Moore's Law
- Leading logic players in early commercial production of 3D hybrid bonded devices for data center CPUs and GPUs
- New photonics use cases emerging utilizing co-packaged optics (CPO) with hybrid bonding
- ASIC usage of hybrid bonding anticipated next year
- HBM4/5 requires most advanced processes including hybrid bonding and TCB Next
- Next generation CoWoS-L/R structures evaluating TCB Next, next gen Flip Chip and MMA solutions

Many New Advanced Packaging Fabs Planned

Approximately $100B investment in progress or planned

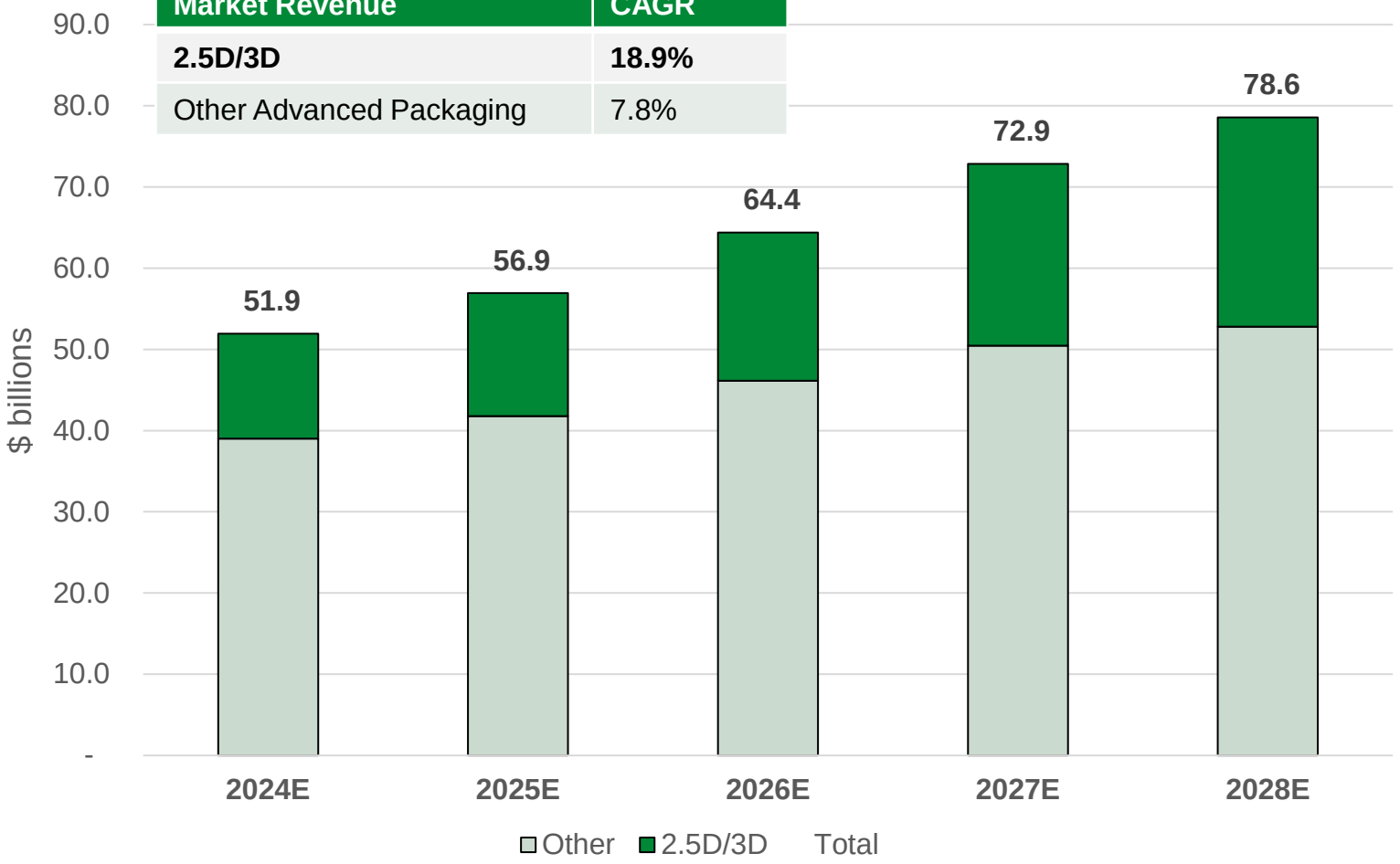
Packaging Fab Project	Initiated	Cost ($B)	Status
TSMC AP7 CoWoS & SoIC - Chiayi, Taiwan	2024	15,0	In Progress
TSMC AP – Arizona, USA	2025	~10,0	Planned
TSMC AP8 CoWoS – Tainan, Taiwan	2024	7,7	In Progress
Intel - Penang, Malaysia	2022	7,1	On Hold
Intel - Wrocław West, Poland	2023	4,6	On Hold
Intel Fab 11x - New Mexico, USA	2021	4,0	Ramping
Intel – Chengdu, China	2025	0,3	Planned
SK Hynix HBM - Indiana, USA	2024	3,9	Planned
SK Hynix M15 Expansion - South Korea	2024	1,0	In Progress
Samsung - Cheonan, South Korea	2024	8,1	Planned
Samsung - Texas, USA	2024	4,0	Planned
Micron - Singapore	2025	7,0	Planned
Micron - Gujarat, India	2023	2,8	In Progress
Micron - Xi'an, China	2023	0,6	In Progress
STMicro – Catania, Italy	2024	5,0	Planned

Packaging Fab Project	Initiated	Cost ($B)	Status
SPIL – Changhua & Yunlin, Taiwan	2025	3,3	In Progress
SPIL P1 - Pulau Pinang, Malaysia	2024	1,3	In Progress
SPIL – Houli Plant, Douliu Plant Taiwan	2024	0,1	In Progress
Silicon Box - Italy	2024	3,6	Planned
Tata TSAT - Assam, India	2024	3,2	Planned
Amkor Technology – Arizona, USA	2024	2,0	Planned
SJ Semi AP – Jiangyin, China	2023	1,4	In Progress
JCET WLP – Jiangsu, China	2024	1,4	In Progress
HT Tech AP – Nanjing, China	2024	1,4	In Progress
TFME AP – Tongda, China	2024	1,0	In Progress
Hana Micron – Vietnam	2025	1,0	Planned
Global Foundries AP – New York, USA	2025	0,6	Planned
Amkor + AICEP – Portugal	2024	0,4	In Progress
Foxconn EU	2025	0,3	Planning
JCET (automotive) - Shanghai, China	2023	0,2	In Progress

Source: TechInsights, Besi May 2025

Advanced Packaging Revenue Forecast to Grow Rapidly 2.5D/3D Fastest Growing Segment

Market Revenue	CAGR
2.5D/3D	**18.9%**
Other Advanced Packaging	7.8%



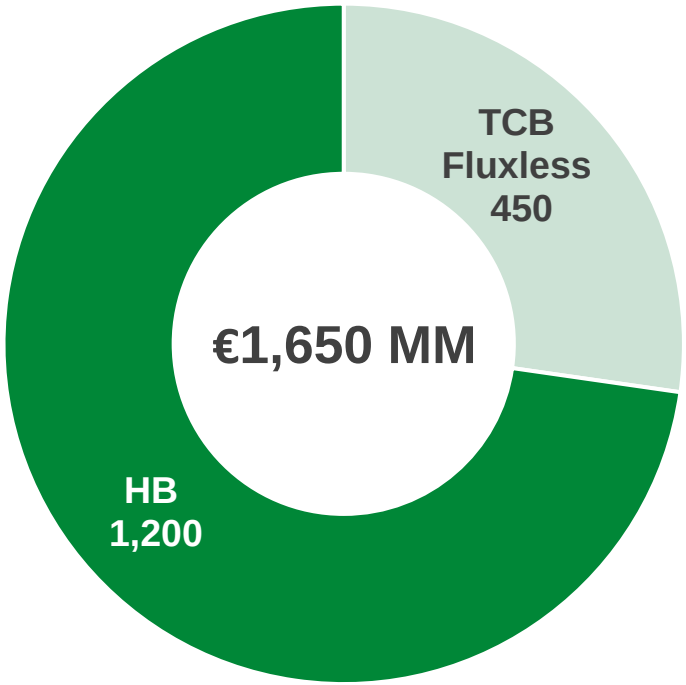
Besi Portfolio Well Positioned by Node Size and Accuracy

- ~70% of Besi equipment revenue from advanced packaging
- ~50% equipment revenue from advanced die placement (< 7 micron accuracy)
- ~50% of revenue AI-related
- Entering Fluxless TCB market

Source: Yole, December 2024

Besi Focuses on Highest Growth Segments of Advanced Packaging

Estimated 2030 Hybrid Bonding & TCB Fluxless Market Size (€ MMs)



Hybrid bonding estimated to be largest assembly segment by 2030

- Assumes transition from TCB to hybrid bonding as from HBM5
- Estimated market size in 2030 =~350 units (mid case)

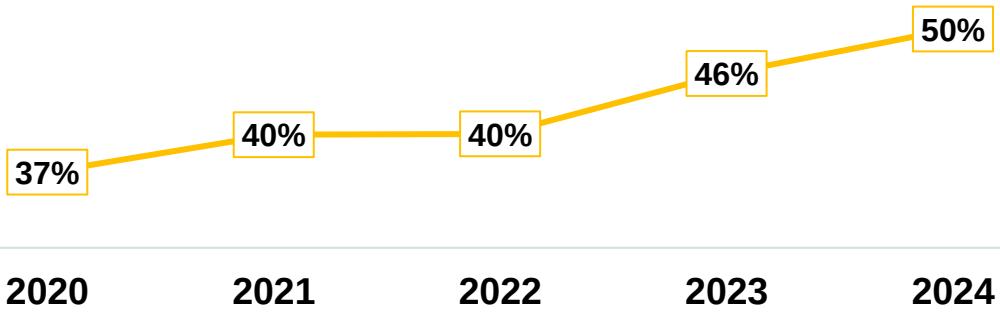
Besi entering Fluxless TCB market

- Emerging market with significant growth potential
- Focused on highest value added advanced chiplet and memory applications
- Estimated market size in 2030=~100 units (mid case)

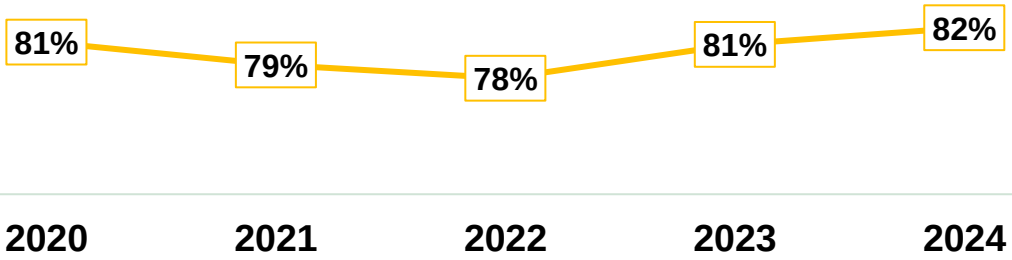
Source: Besi estimates. Mid case scenario hybrid bonding

Besi's Die Attach Market Share Trends

Die Attach[1]



Advanced Die Placement[1,2]



Source: TechInsights, June 2025

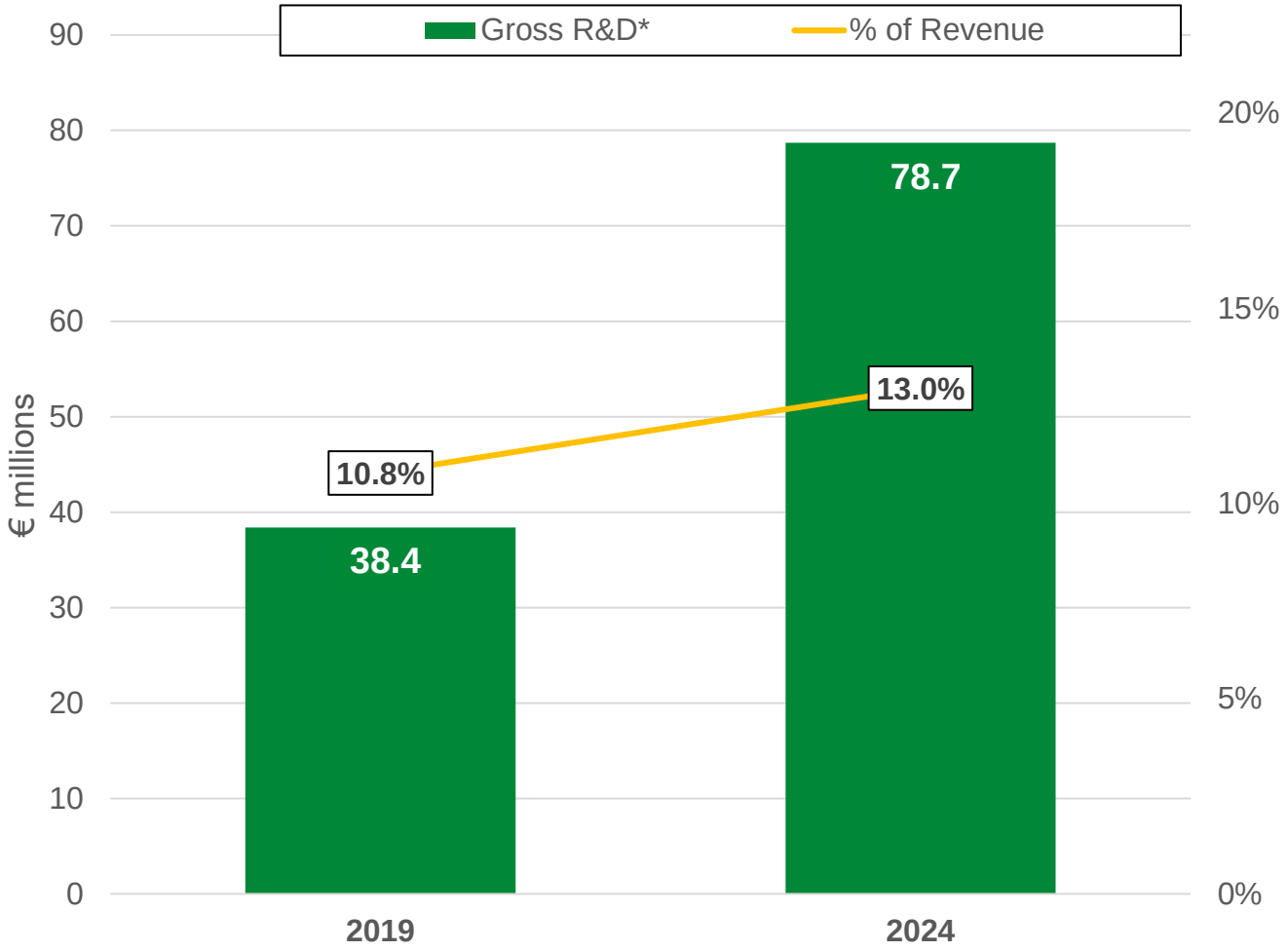
1) Excludes TCB, wire bonding, dicing, and other
2) Advanced die placement defined as < 7 micron accuracy per TechInsights

Summary Strategy

Strategic focus/discipline has been a winning formula:

- Maintain position as R&D leader
- Focus on advanced packaging
- Win with the winners
- Seek profit over market share
- Provide leading-edge systems at mainstream cost structure and lead times
- Keep highly flexible and scalable production model
- Grow in sustainable manner

Expansion of R&D Spending in Support of New Product Introductions



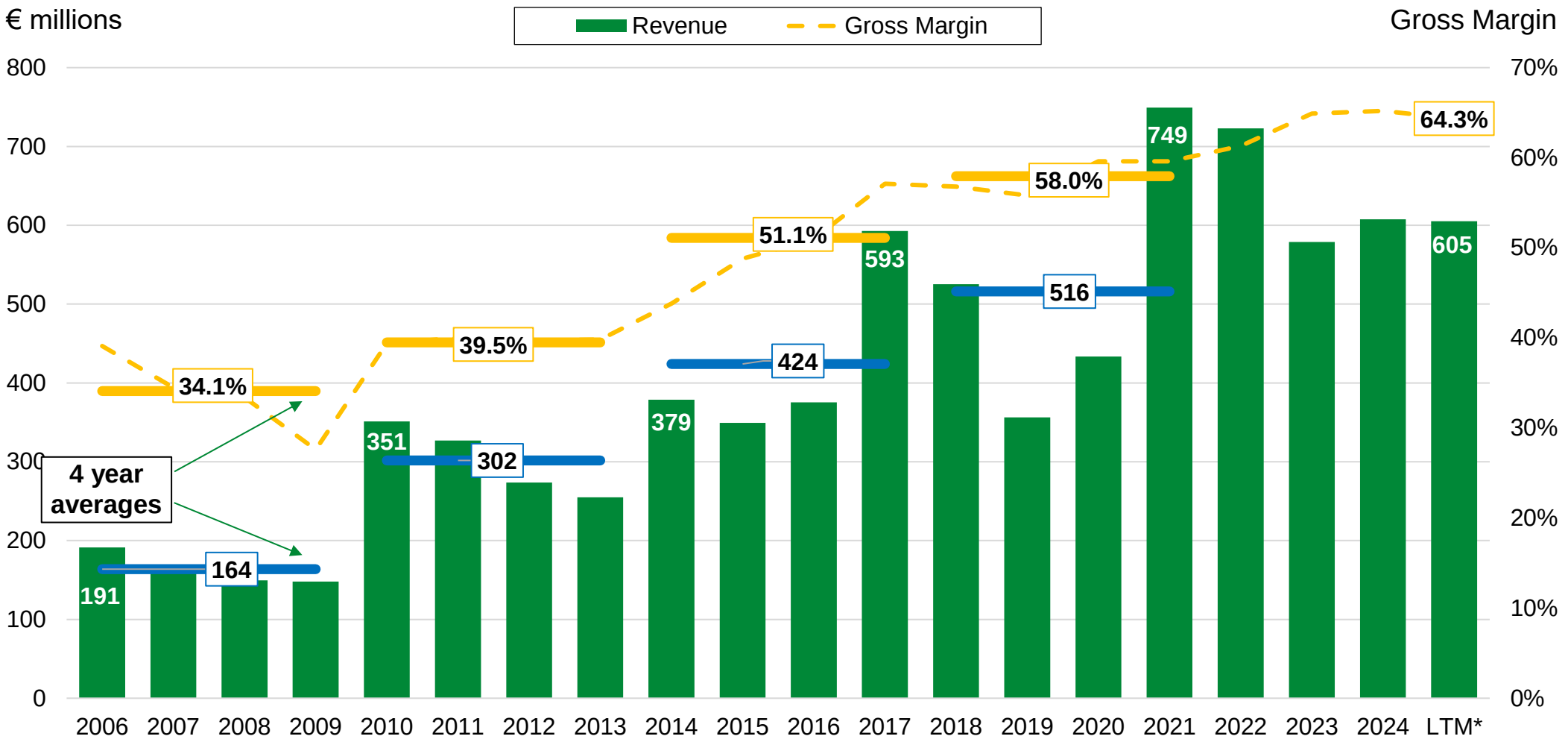
* Gross R&D spending excludes impact from capitalization/amortization of R&D costs

Innovation is a key driver of our business:
- New opportunities for each next-generation advanced packaging system

Significant R&D investment in advanced packaging over past 5 years to support:
- New 2.5D/3D IC assembly structures for AI
- Portfolio enhancements for next market upcycle

Key areas of current focus:
- 50 nm accuracy hybrid bonder
- TCB Next for memory and logic applications
- Advanced CoWoS:
  - 1 micron accuracy Evo
  - Next gen flip chip

Higher Through Cycle Revenue and Gross Margins

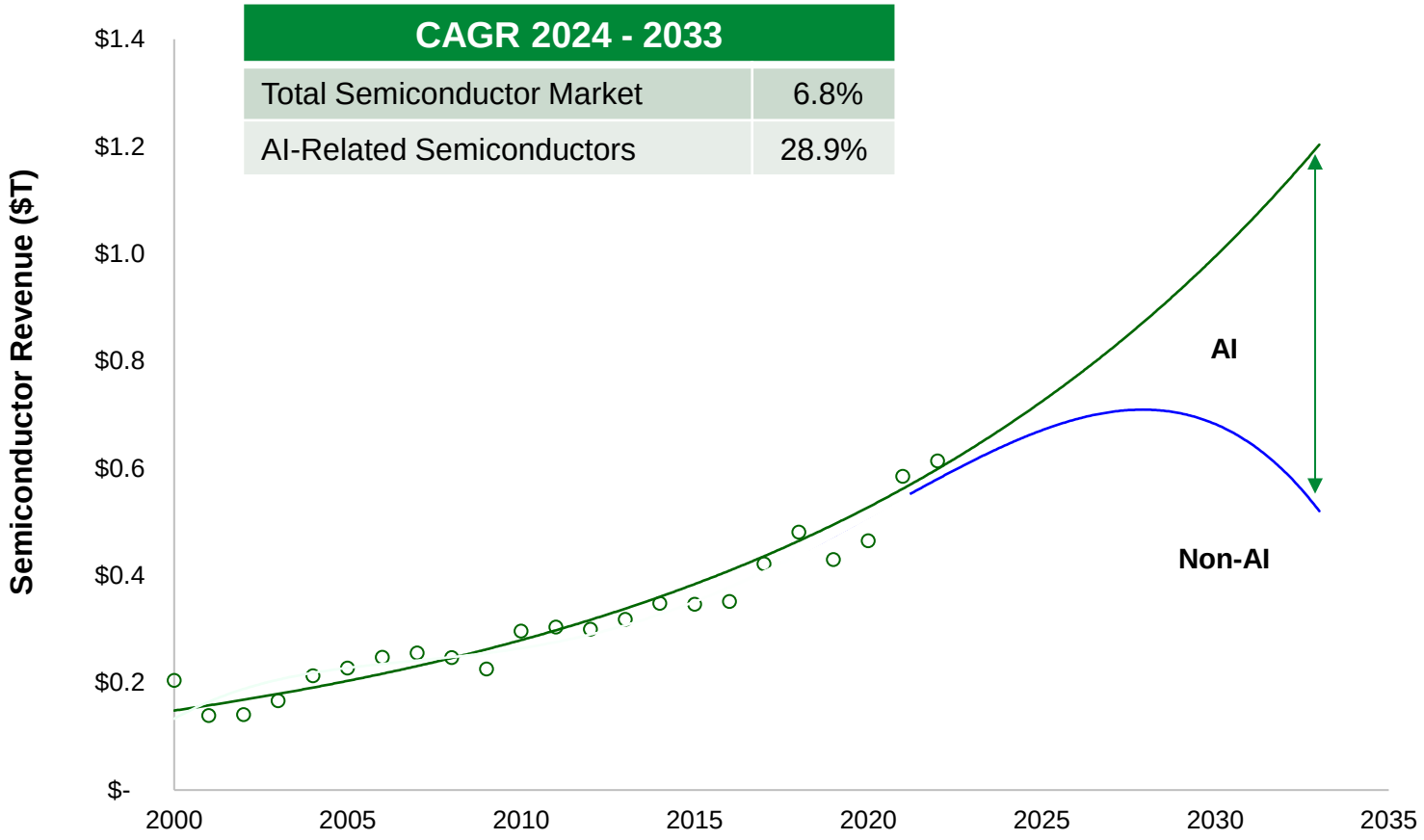


* LTM per Q1-25

II. MARKET TRENDS
Chris Scanlan
Senior VP Technology

AI is Driving Long-Term Semiconductor Revenue Growth

CAGR 2024 - 2033	
Total Semiconductor Market	6.8%
AI-Related Semiconductors	28.9%



Sources: TechInsights 2025, Precedence Research Nov 2024


Humanoid Robotics


Autonomous Taxis


AI Wearables (AR/VR)


AI Smartphones


AI Personal Computers


Data Center AI Infrastructure

And Growth in Besi's Principal End-User Markets

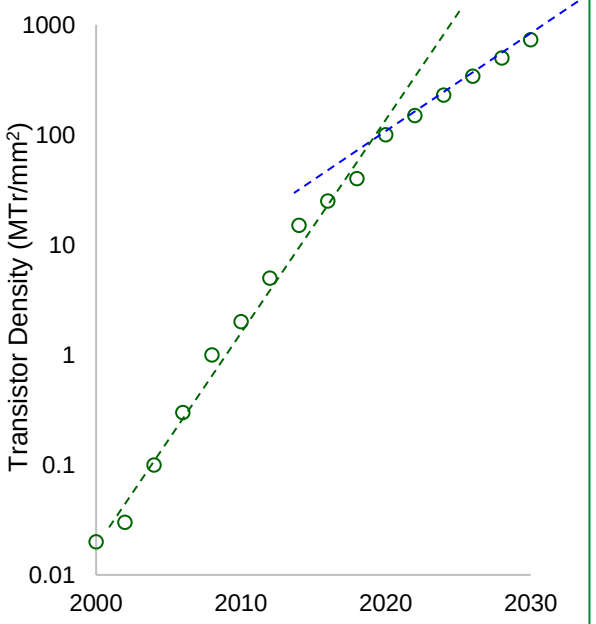
Computing (43%)	Mobile Internet (20%)	Automotive (12%)	Industrial/Other (9%)
			
Agentic AI	**AI Smartphone**	**Autonomous Driving**	**Robotics**
Training and Inference AI Enabled PC Si Photonics	AR/VR Headsets Camera Technology 5G Advanced → 6G	Vehicle Electrification Connectivity Infotainment	Smart Grid Industrial IoT Clean Energy

Percentages based on 2024 estimated revenue per end market application. Spares/service revenue was ~16% of 2024 revenue

Slowing of Moore's Law Accelerates Adoption of Chiplets & 3DIC

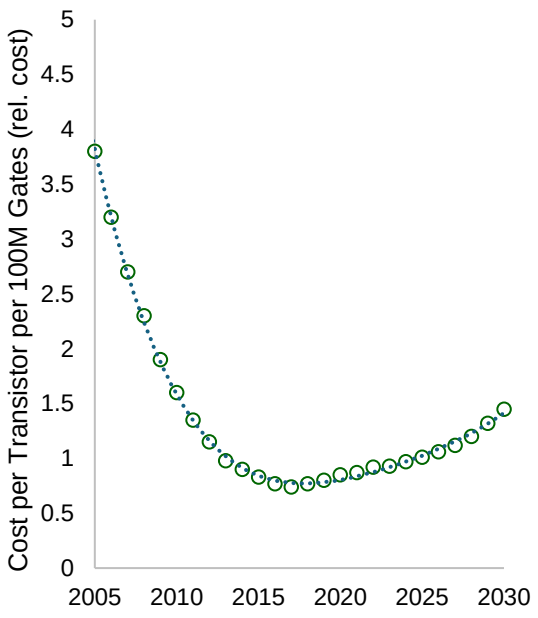
- **Moore's Law slowing** as data volumes grow exponentially and commercial applications expand
- **Customers adopting chiplets**, connected via hybrid bonding and TCB, to optimize device function per node and reduce cost

Transistor Density Slowing



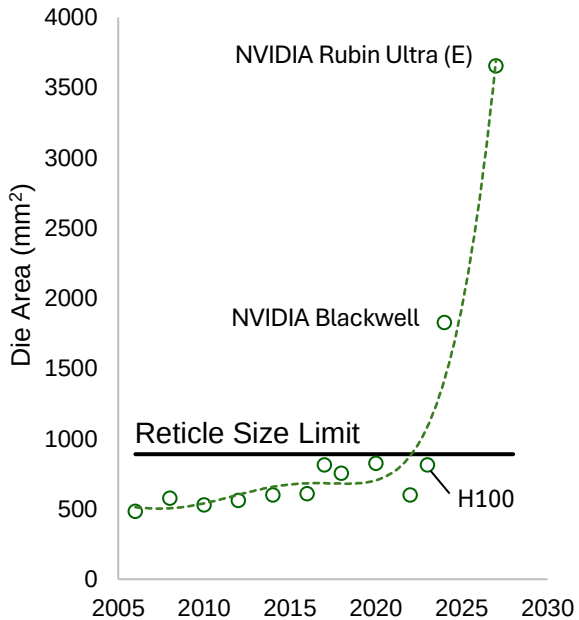
Source: IRDS 2023 Edition

Cost per Transistor Increasing



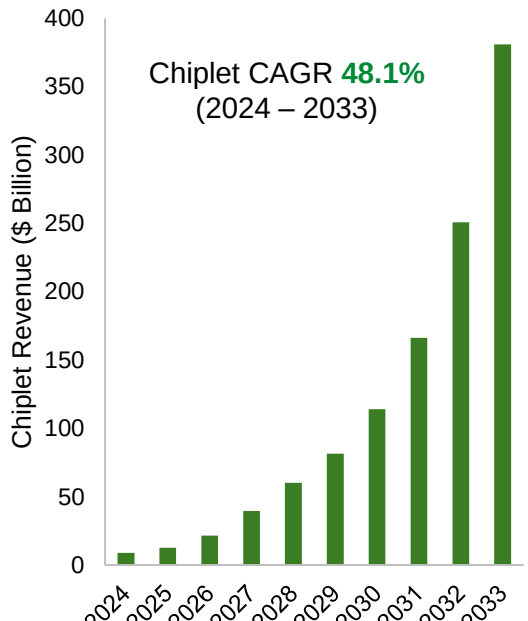
Source: Tom's Hardware, IEDM 2023 - Google

Die Sizes Exceeding Reticle Limits



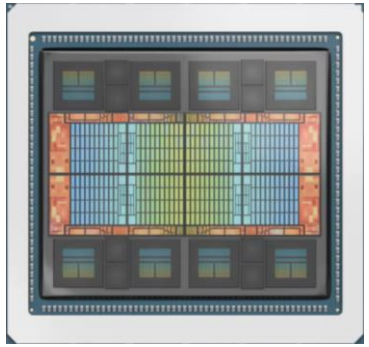
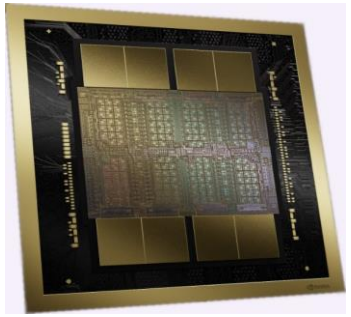
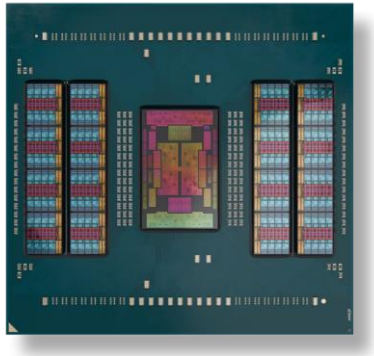
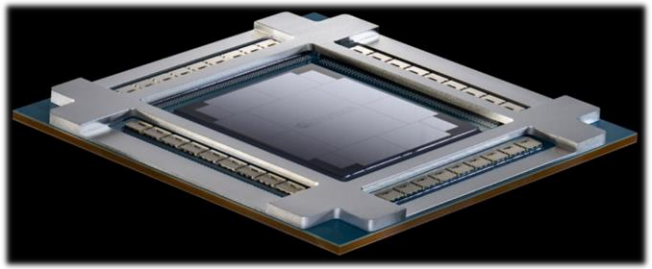
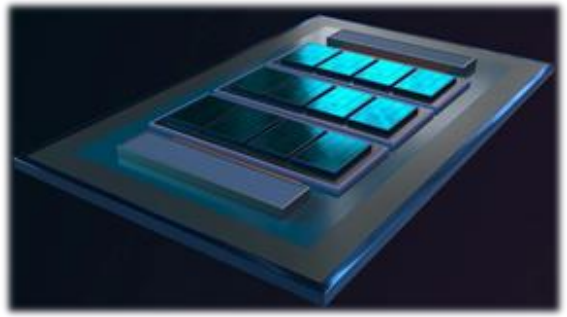
Source: Besi

Chiplet Usage Expected to Grow Rapidly



Source: Dimension Market Research January 2025

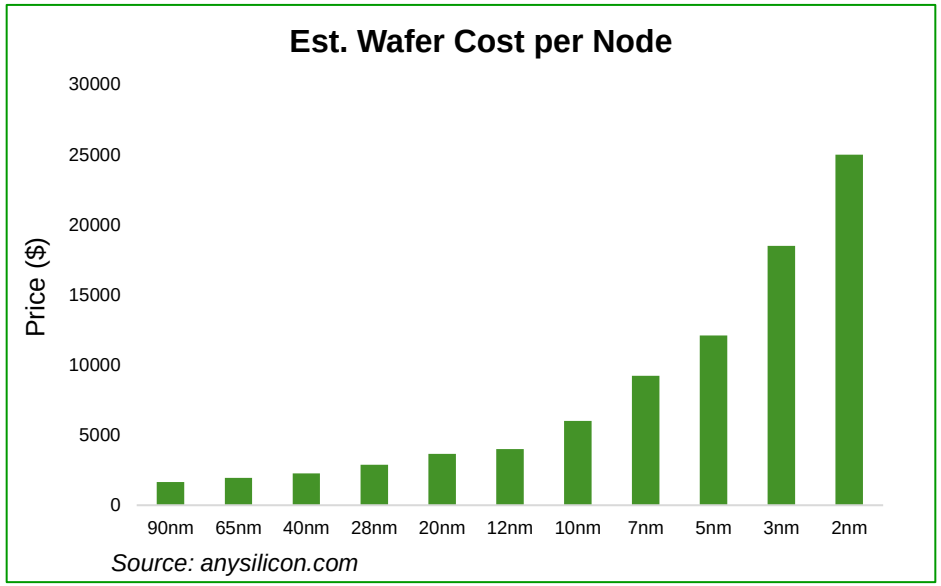
Latest Advanced Data Center Chips Adopting Chiplet Architectures

AMD	NVIDIA	Intel
MI325 GPU  CoWoS-S (**Hybrid Bonding)**	**B100 (Blackwell) GPU**  CoWoS-L package	**Gaudi 3 AI Accelerator**  CoWoS-S package
Zen 5 EPYC CPU  SoIC (**Hybrid Bonding**)	**Spectrum X Network Switch**  CoWoS-S with CPO (**Hybrid Bonding)**	**Clearwater Forest CPU**  Foveros Direct (**Hybrid Bonding**)

AMD Demonstrating Value of Chiplets Across CPU Roadmap

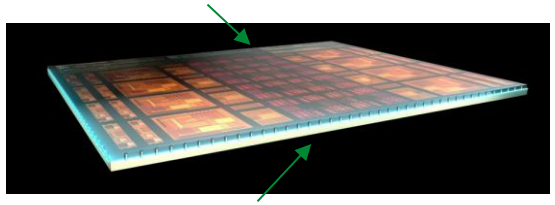
- **Escalating cost with each new advanced node**

- **Chiplet benefits**:
  - Improved yield and cost efficiency
  - Increased energy efficient performance
  - Increased design flexibility
  - Faster time to market
  - Scalability



AMD Zen5 3D CCD Chiplet using **Hybrid Bonding**

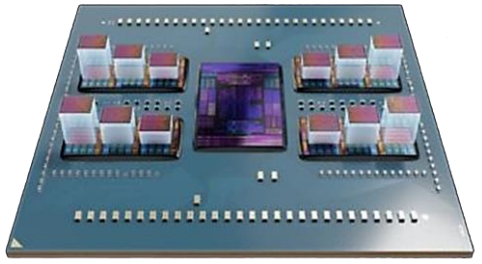
Compute chiplet on top



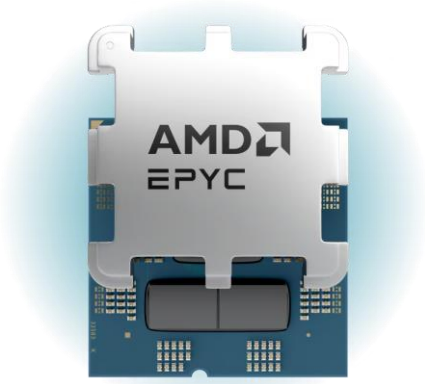
SRAM chiplet on bottom

Source: AMD

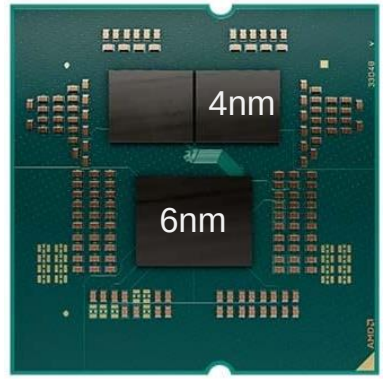
AI Data Center
EPYC 9004 Series



General Purpose Server
EPYC 4585PX

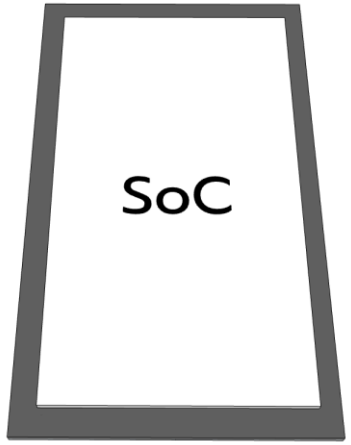


Gaming PC
Ryzen 9 9900X3D



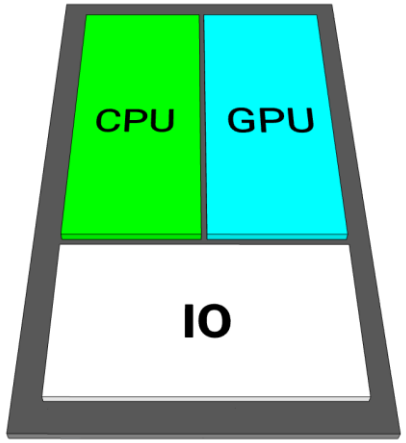
Chiplet Usage Also Drives Demand for Advanced Die Attach Equipment

Single Chip Design



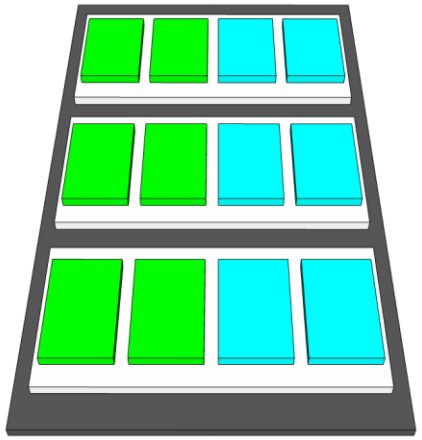
Monolithic: Integrated SoC

Multi Chip Module



Multiple Dies: node optimized

3D Multi Chiplet System



Individual IPs: node optimized

1	Die attach steps	Dozens
10µm	Accuracy	100nm

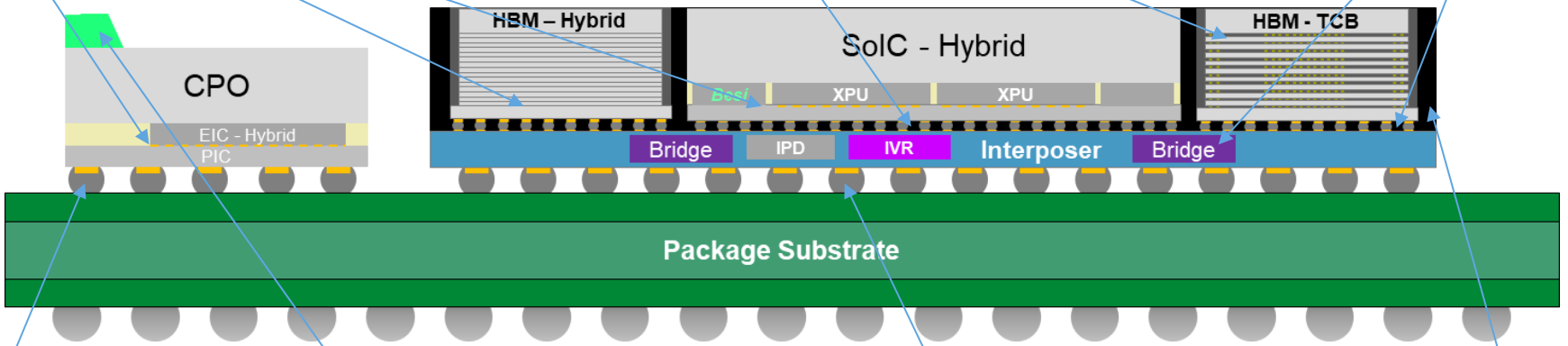
Source: Intel

AI Chiplet Packages Require a Variety of Advanced Packaging Solutions

Hybrid Bonding
3DIC stacking < 9µm pitch
HBM stacking ≥ 16 High
Photonics

Thermo-compression Bonding
C2W chiplet stacking
HBM stacking ≤ 16 High
3D bridge attach

CoW Flip-chip and Fan-out
CoW flip-chip of logic & memory
High-density fan-out
Embedded bridge die attach



Flip-chip CoS
Advanced mass reflow flip-chip attach > 40 um pitch

Photonics
High precision optical component placement

Interposer Attach
oS bonding of large interposers up to 110 mm

Chiplet Molding
CoW encapsulation
CoWoS molded underfill

Besi Developing Complete Portfolio for Complex AI Chiplet Packages

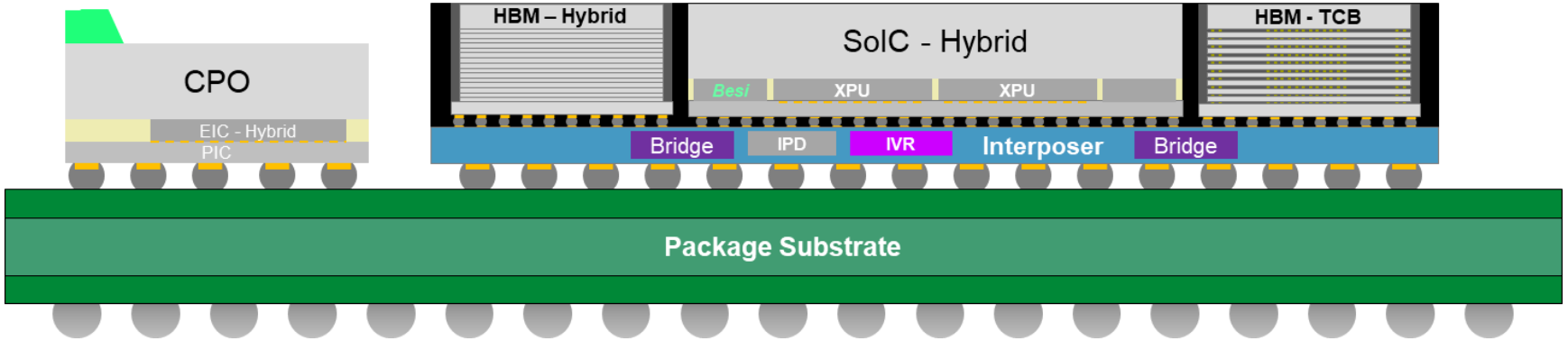
Hybrid Bonding
8800 CHAMEO UltraPlus AC

Thermo-compression Bonding
9800 TC Next

New

CoW Flip-chip and Fan-out
8800 CHAMEO fleX

Q1-26



New

Flip-chip CoS
8800 Quantum AdvX

Q1-26

Photonics
2200 evo 1µm

Interposer Attach
2200 evo Advanced

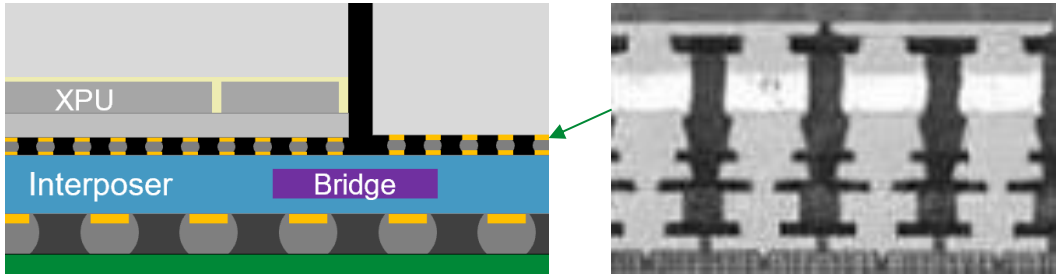
R&D

Chiplet Molding
xMS-NXT

Hybrid Bonding is Technology of Choice for High Performance Logic Chiplet Stacking

TCB Micro-bump C2W

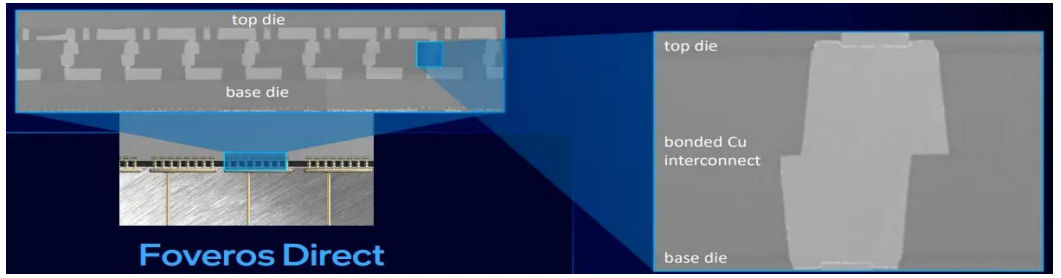
TCB C2W used for lower density, less performance critical applications, such as CoW interposer assembly



Source: INTEL

Hybrid Bonding

Highest performance interconnect to create 3D ICs in front-end wafer fabrication process



Source: INTEL

Micro-bump C2W TCB	Performance Factor*	Hybrid Bonding
1X	**Interconnect Density**	**15X**
1X	**Speed**	**11.9X**
1X	**Bandwidth Density**	**191X**
1X	**Energy Efficient Performance, EEP****	**>100X**
10X	**Cost per Interconnect*****	**1X**

Data source: * TSMC 2023, ** TSMC 2025, ***Besi estimate based on max interconnect density

Intel Introducing New Products Using Hybrid Bonding

Intel using hybrid bonding to stack CPU core chiplets atop base tiles with SRAM and I/O functions

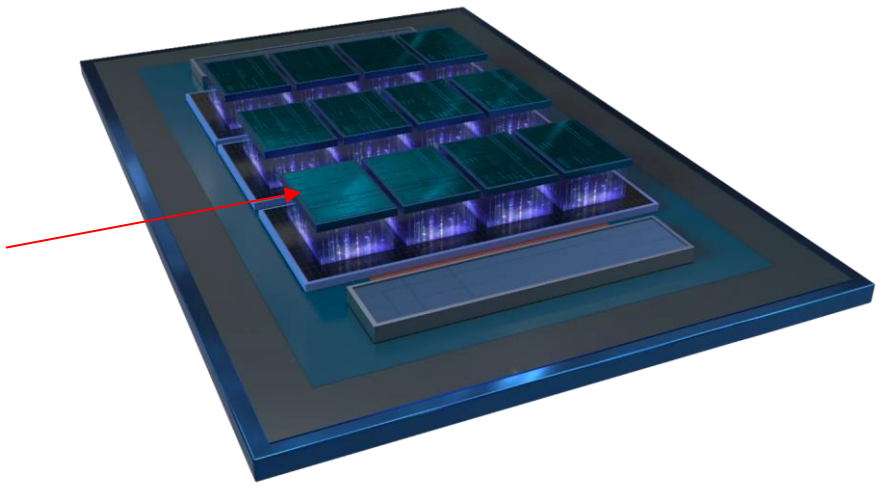
3D stacking "***improves the latency between compute and memory by shortening the hops, while at the same time enabling a larger cache***" - Pushkar Ranade, Intel

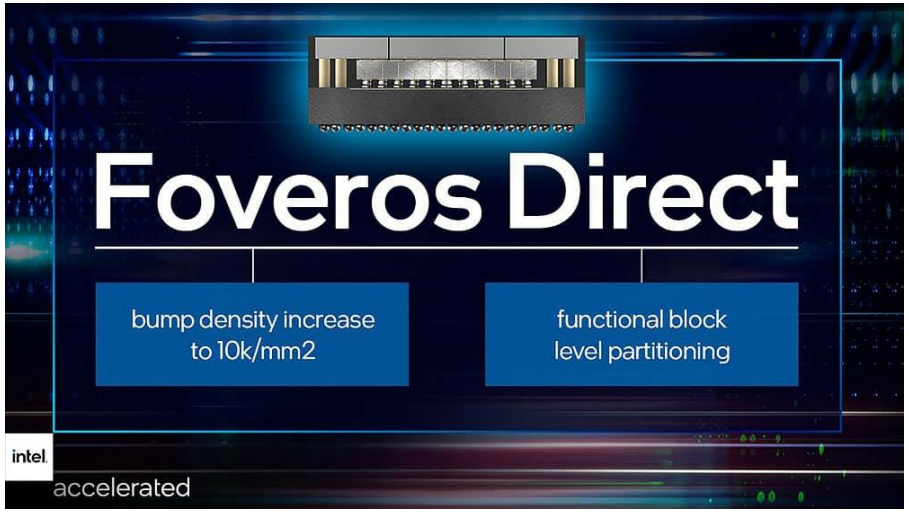
Clearwater Forest Data Center CPU (2025)

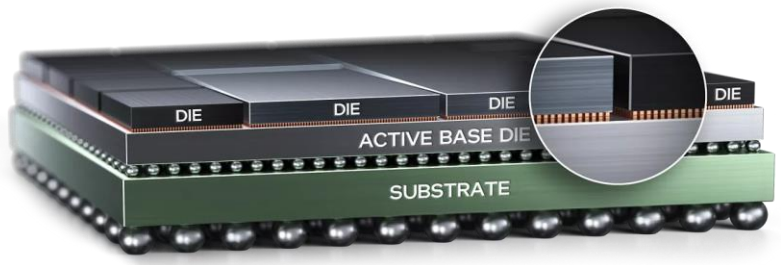
12 CPU chiplets on Intel 18A node

3D stacking of CPU chiplets to base die using **hybrid bonding**

Total 300 billion transistors







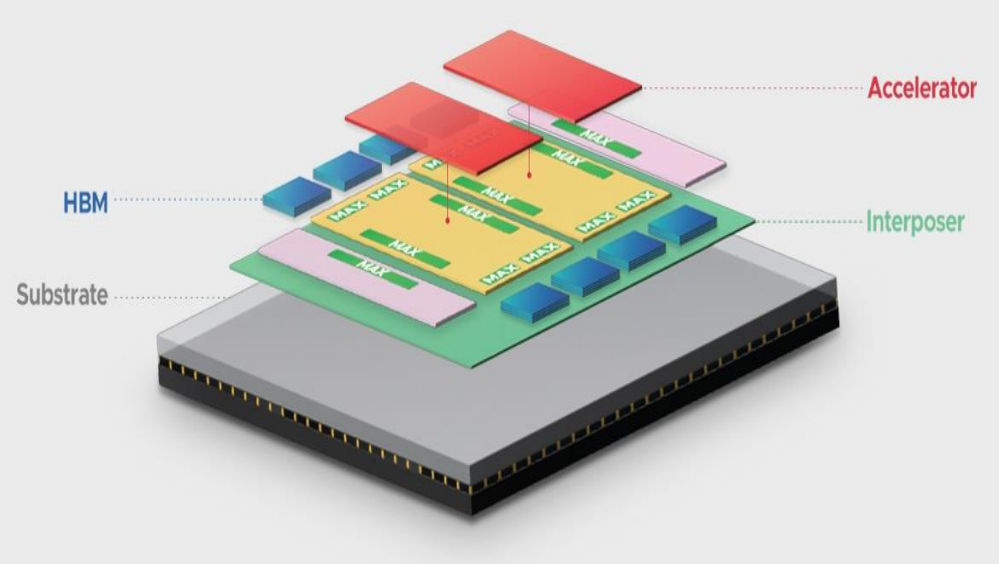
Source: Intel

New Hybrid Bonding Applications Expected to Ramp in Near Term

Broadcom Delivers Industry's First 3.5D F2F Technology for AI XPUs

Combination of 3D silicon stacking and 2.5D packaging technology enables custom compute platforms with breakthrough performance, power and cost

- Broadcom co-develops AI chips for customers such as Google, Fujitsu, Apple and Open AI
- Announced use of hybrid bonding for custom AI ASICs
  - Using TSMC's SoIC process with face-to-face hybrid bonding
  - Initially at 6 micron bond pad pitch
- Production estimated to begin in 2026



Source: Broadcom

M5 Pro chip could separate CPU and GPU in 'server grade' chips

Ben Lovejoy | Dec 23 2024 - 7:03 am PT | 8 Comments

The M5 series chips will adopt TSMC's advanced N3P node, which entered the prototype phase a few months ago. M5, M5 Pro/Max, and M5 Ultra mass production is expected in 1H25, 2H25, and 2026, respectively.

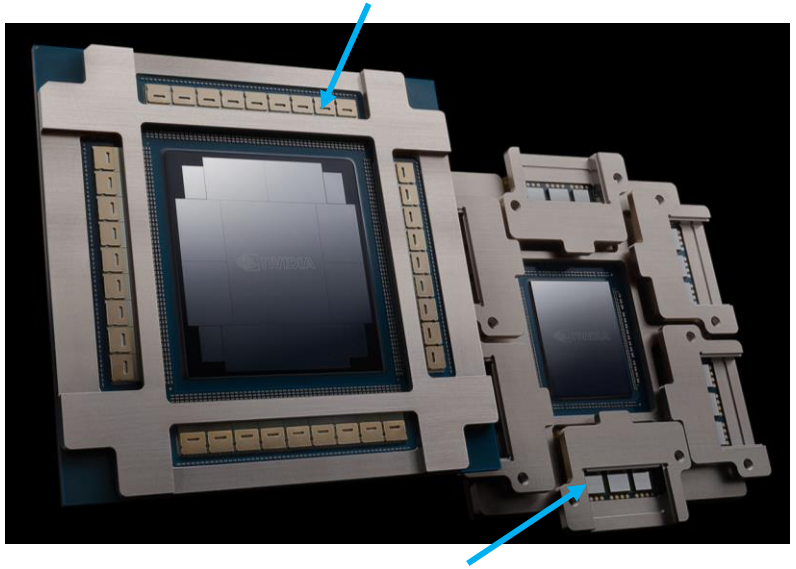
The M5 Pro, Max, and Ultra will utilize server-grade SoIC packaging. Apple will use 2.5D packaging called SoIC-mH (molding horizontal) to improve production yields and thermal performance, featuring separate CPU and GPU designs.

Source: https://9to5mac.com/2024/12/23/m5-pro-chip-could-separate-cpu-and-gpu-in-server-grade-chips/

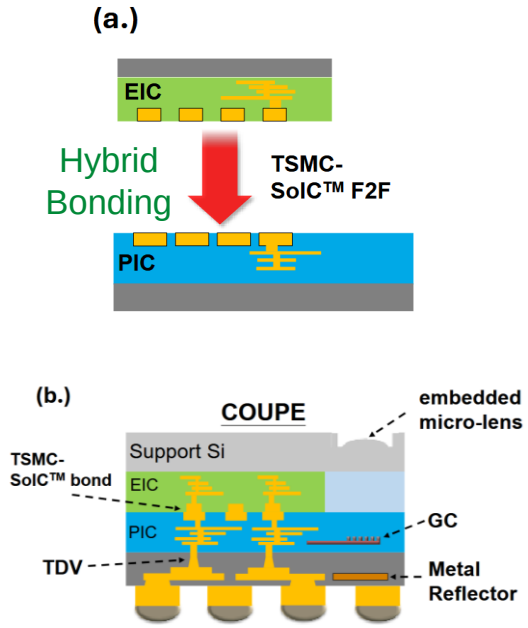
CPO Use Cases Emerging in New Product Announcements

NVIDIA using hybrid bonding in new network switch products using co-packaged optics (CPO)

Spectrum-X™ Ethernet switch with 36 CPO chiplets



Quantum-X800 InfiniBand switch with 18 OE chiplets



Source: TSMC, ECTC 2025

- Based on TSMC's COUPE technology that uses hybrid bonding
- Up to 36 hybrid bonded chiplets per switch device
- Should help drive significant hybrid bonding capacity expansion through 2030

Broadcom's CPO network switches utilize multiple advanced flip-chip bonding processes

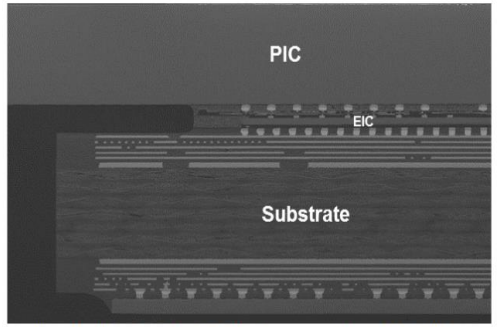
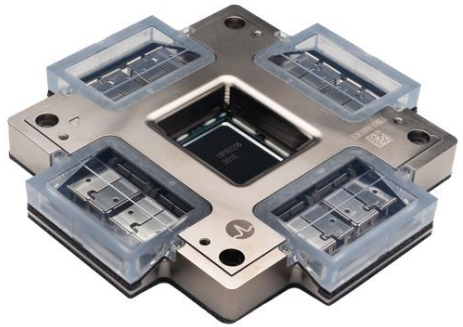
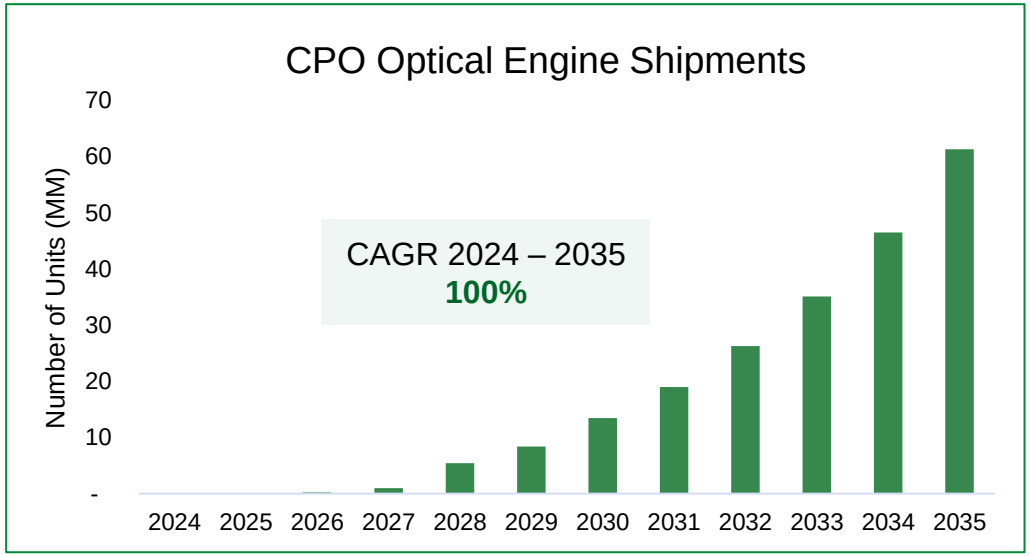


Fig. 9. The x-section of OE structure after TCN 500X



Source: Broadcom

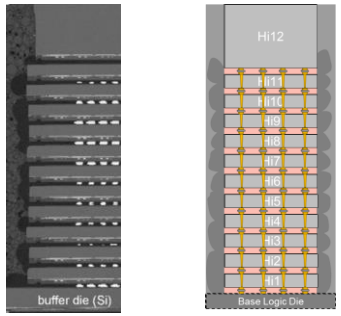


Source: Yole CPO 2025

HBM Bonding Technology Roadmap and Besi´s Opportunity

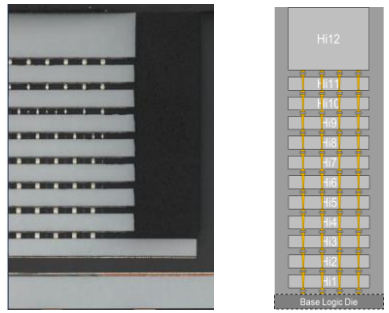
Well positioned to win in TCB with highest accuracy, quality and productivity
Orders from 3 major logic and memory customers and IMEC

TCB-NCF



Source: TechInsights

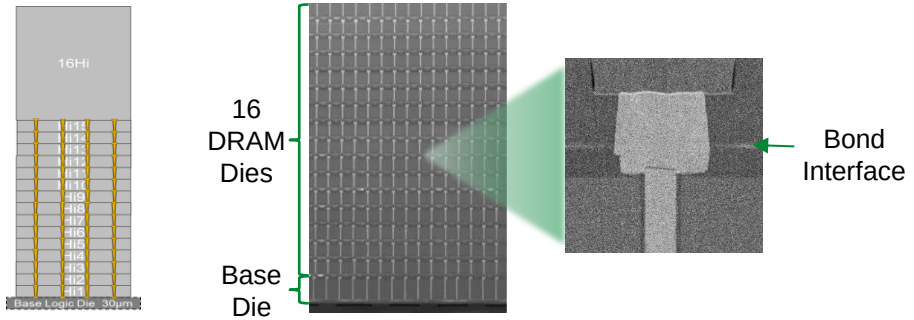
Fluxless TCB-MUF



Source: SKHynix

Leading integrated hybrid bonding system for HBM stacking
Orders from 2 major memory customers

Hybrid Bonding



Source: Samsung

		HBM3	HBM3e	HBM4	HBM4e	HBM5
Year of Release		2023	2024	2025	2026	2028
Besi Opportunity				**C2W TCB**	**Hybrid Bonding**	
# of Dies	**TCB**	8	12	16	16	-
	Hybrid				16	**≥20**
Interconnect Pitch		25µm	22µm	20µm	18µm	**<15µm**
Base die technology		≥12nm IDM buffer die		**≤ 4nm advanced foundry logic**		

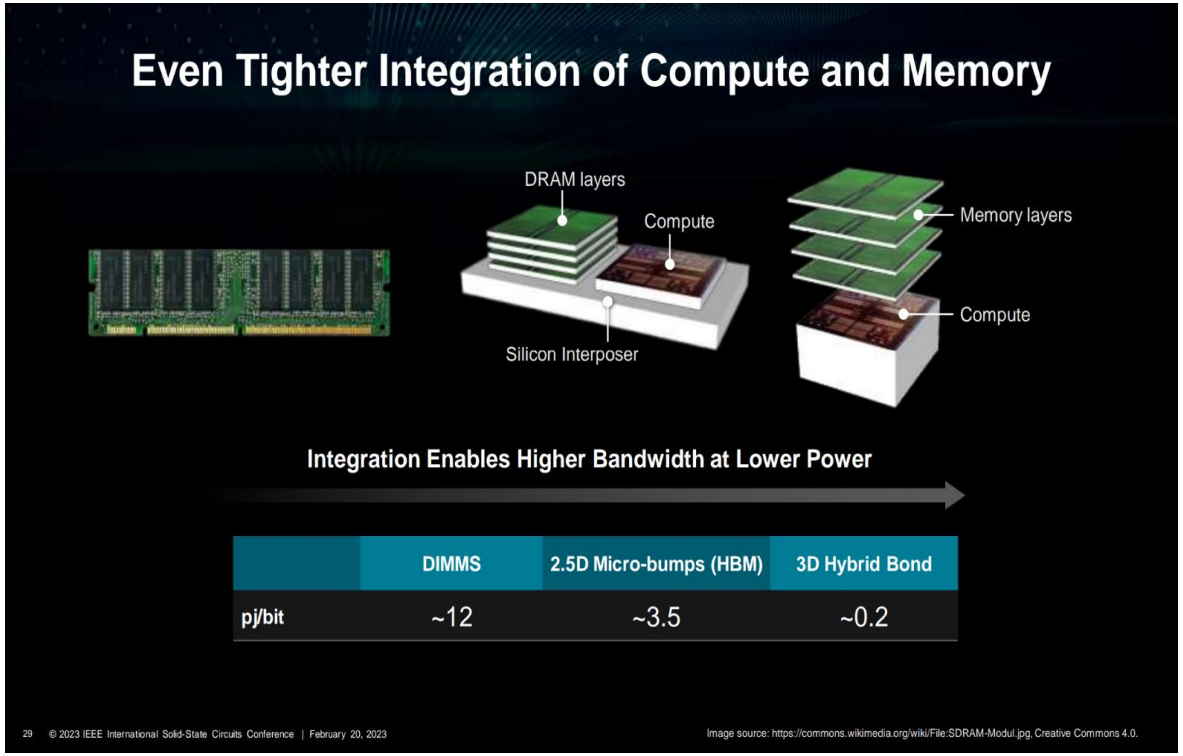
* NCF = non conductive film ** MUF = molded underfill

Hybrid Bonding Enables Next Generation HBM to Incorporate Higher Performance, Custom Logic Base Die

Use of advanced logic nodes for the HBM base die is planned from HBM4 onwards

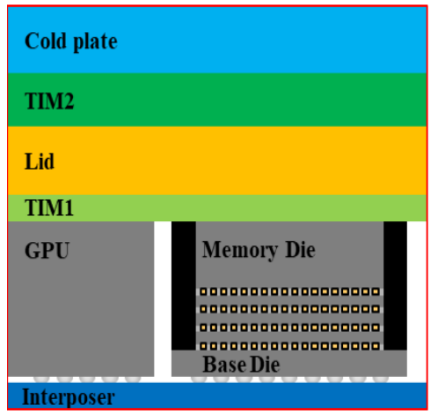
- Additional compute functionality will be added to the base die, increasing thermal power dissipation requirements
- Hybrid bonding necessary to overcome the thermal performance bottleneck to enable higher logic power density

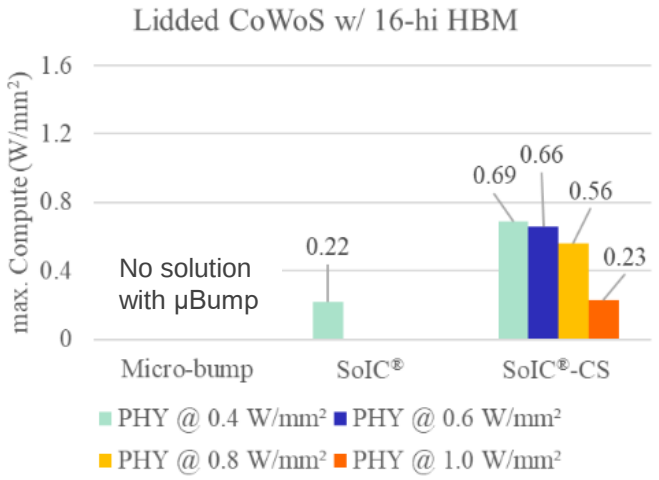
"Micro-bump is not capable of providing decent design flexibility for any ambitious next-generation HBM." – TSMC[1]



Source: AMD

Hybrid bonding with enhanced interface layer reduces thermal resistance by 4x and improves EEP by >100x compared to µbump.[1]





[1] Source: "Innovative SoIC® Cool-Stacking Technology to Overcome the Thermal Wall of Future High-Performance Compute" TSMC, 2025 ECTC

AI Enabled Smartphones Also Expected to Adopt Chiplet Solutions

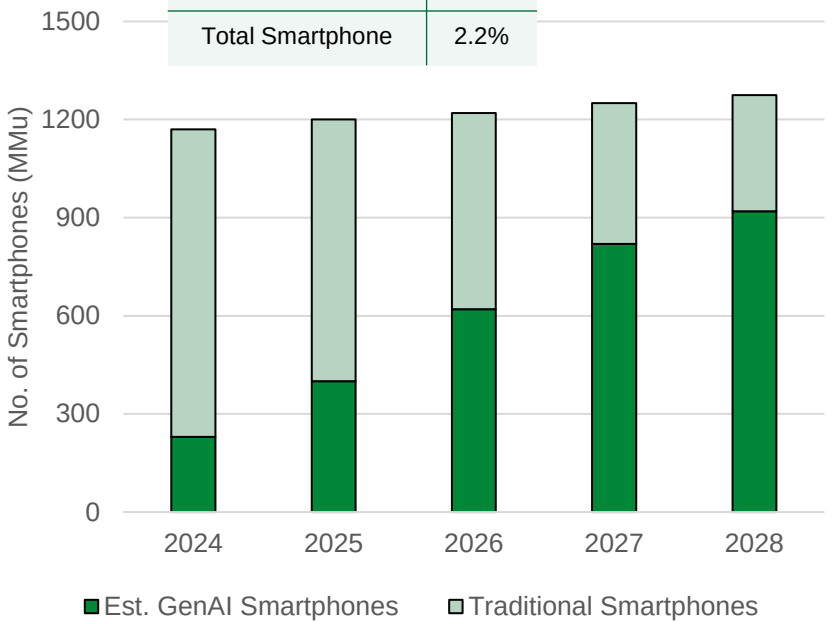
GenAI enabled smartphone market expected to grow at 41.4% CAGR 2024-2028

- Will require processors with more NPU power and more memory with higher bandwidth connection to the APU
- Adoption of chiplet architectures for the APU and new memory packaging to fit more chips in the same vertical space

AI enabled phones will require 2.5D and 3D chiplets assembled on wafer level using flip-chip, TCB and hybrid bonding

- Should drive major upgrade cycle for APU packaging with opportunities for Besi's CHAMEO *fleX*, TC Next and hybrid bonding

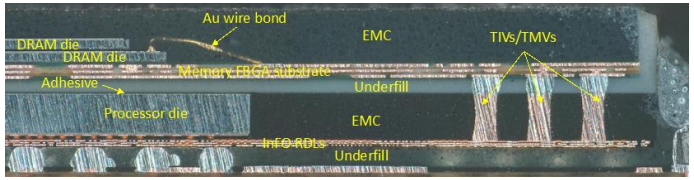
CAGR 2024 – 2028E	
Gen AI Smartphone	41.4%
Total Smartphone	2.2%



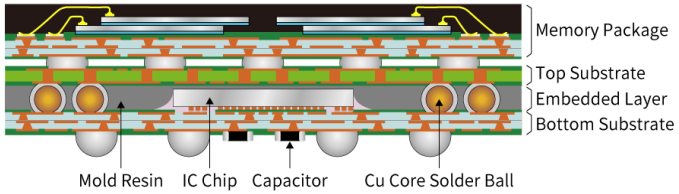
Source: IDC July 2024, TSMC

Current Mobile APU with Single SoC

InFO PoP (Apple A18)



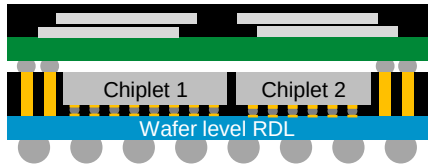
MCeP (Qualcomm, Mediatek, HiSilicon)



Source: Techsearch

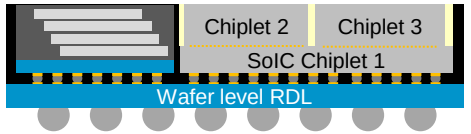
Future Chiplet APU Devices with Wafer Level Assembly (2027-28E)

CoW-R

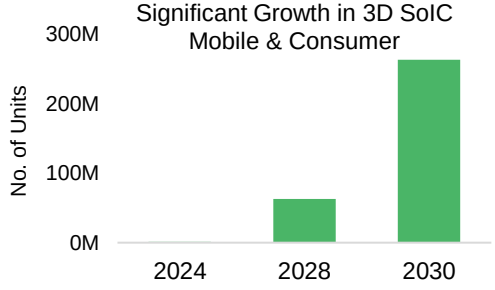


8800 CHAMEO *fleX* CoW

SoIC X/P



Hybrid Bonding, TC Next



Source: Yole May 2025

Summary

Rapid advancements in AI technology and applications **driving growth in all Besi end-user markets**
Besi's R&D focused on providing 2.5D and 3D interconnect solutions for high performance AI enabled devices
Accelerating adoption of chiplet architectures as Moore's Law slows
Hybrid bonding is highest-performance, most energy-efficient interconnect technology with lowest cost-per-interconnect
TCB C2W is an emerging process technology with significant market potential
Besi is well positioned to win market share as the high-end assembly market evolves

III. WAFER LEVEL ASSEMBLY

Peter Wiedner

Senior VP Sub-Micron Die Attach

Sub-Micron Die Attach Product Portfolio

Hybrid

2026 8800 CHAMEO ultra plus AC
8800 HYBRID G2

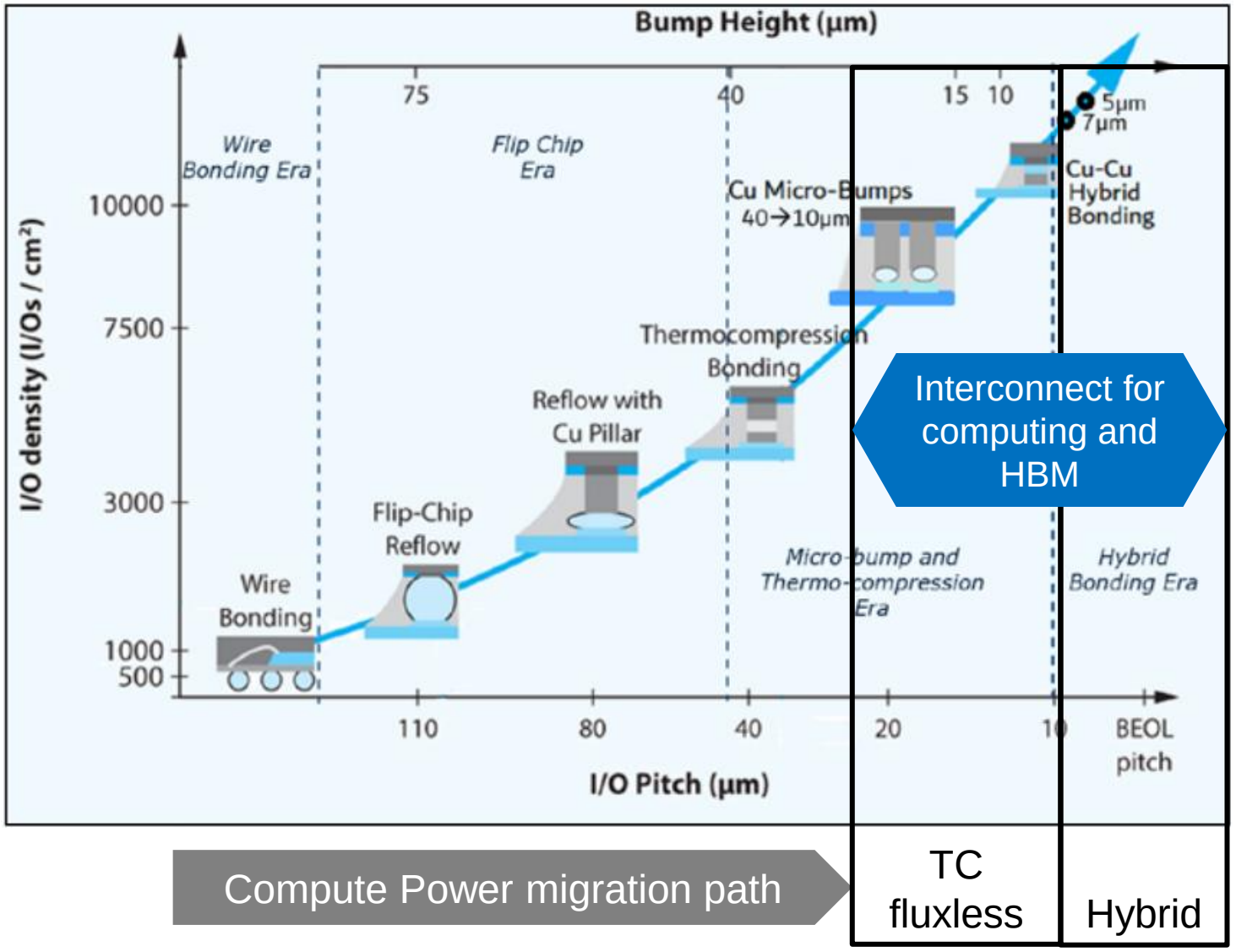
Thermocompression

New 9800 TC *NEXT*

Lid Attach

New DLA Line
TGB hp

Advanced Logic Driving New Fine Pitch Interconnect Technologies

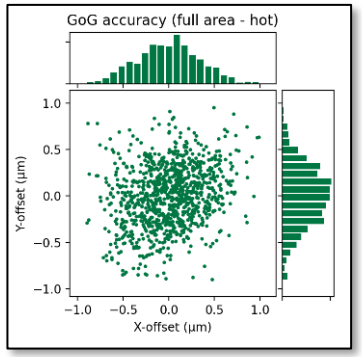


- High end semiconductor design following path to tightest interconnect pitch
  - Hybrid bonding enables bump pitches <10µm
  - Hybrid bonding facilitates 3D chip designs to extend Moore's law
- TCB fluxless bridges gap between existing flux-based TCB and hybrid bonding interconnect
- **Besi strategic focus on leading edge hybrid bonding and TC Next**

TC next – Leading TC Bonder for Next Generation Heterogeneous Integration – Designed for Bump Pitches below 10µm

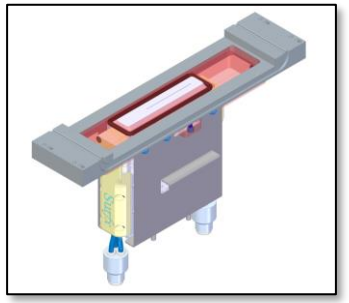
1 Highest Accuracy in Market

Accuracy: 0.7µm



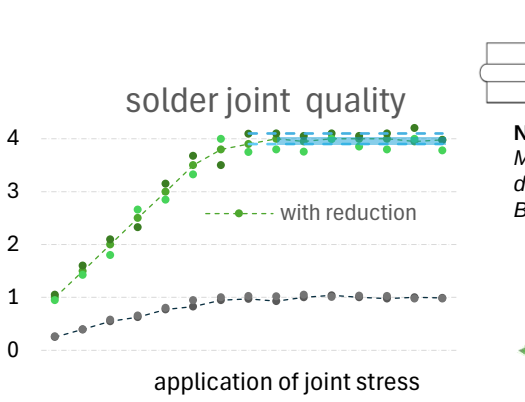
Bump Pitch: 7-20 µm

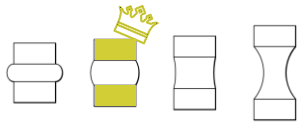
2 Best in Class Fluxless Capabilities



Micro inert chamber and plasma oxide reduction

3 Defense: Realtime Process Control for Each Individual Bond

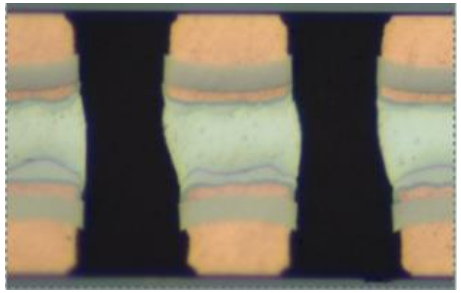




Note:
Model & measurement data based adjustment of BLT / bump shape

4 Best in Class Performance and CoO

UPH up to 2,000

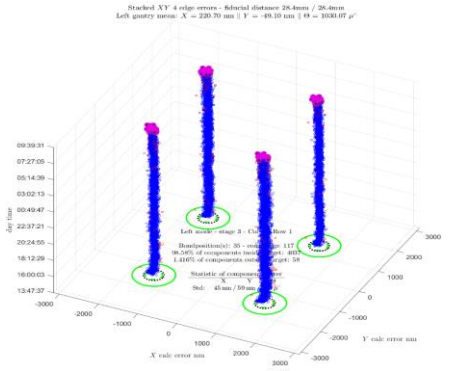


Besi Hybrid Bonder – Highest Accuracy and Lowest CoO

1 8800 CHAMEO ultra plus AC
Today's Industry Standard

Bump Pitch: 6µm

Alignment Accuracy: 100nm



Logic roadmap – driven by accuracy

2 8800 HYBRID G2
Launch in 2026

50nm accuracy enables even smaller pad pitches

Bump Pitch: 3µm

Accuracy 50nm

Significantly higher UPH decreases CoO for HBM

Die stacking UPH: 3,000

3 Roadmap to 25nm and beyond

- Development for 25nm and beyond ongoing
- Enabling transistor to transistor interconnect at 1µm pad pitch by 2030

Bump Pitch: 1µm

4 Improving HBM CoO

- Increasing UPH further to enable cost effective stacking ≥16 high

Die stacking UPH: >5,000

Memory roadmap – driven by throughput

Hybrid Bonding Will Become Mainstream Advanced Packaging Solution

Perception: *Hybrid bonding is too expensive for widespread adoption*

Micro-bump C2W TCB	Performance Factor	Hybrid Bonding
1X	Interconnect Density	15X
1X	Speed	11.9X
1X	Bandwidth Density	191X
1X	Energy Efficient Performance, EEP	>100X
10X	Cost per Interconnect*	1X

Reality:

HB provides superior cost:

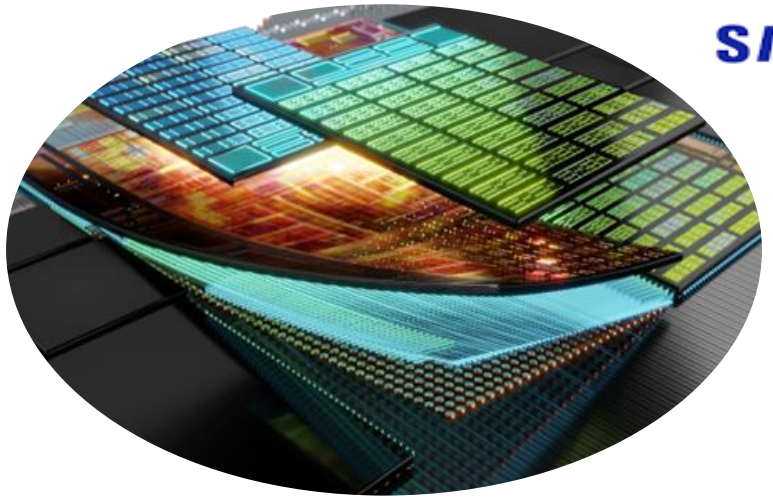
- Requires higher infrastructure cost but delivers 10x lower cost per interconnect
- Increases energy-efficient device performance by >100x, lowering data center operating cost
- Reduces HBM stack temperature by 20%, lowering system cooling cost
- Provides flexibility to combine most cost-efficient silicon nodes
  - First commercial product with hybrid interconnect was a consumer-oriented gaming CPU (AMD Ryzen)

In addition:

HB essential to semiconductor and system design progress:

- Enables more energy-efficient performance and the extension of Moore's law
- Enables HBM roadmap and tighter integration of optical and mixed signals

Application Drivers: AI Logic



SAMSUNG

tsmc

intel

Meta

AMD

Microsoft

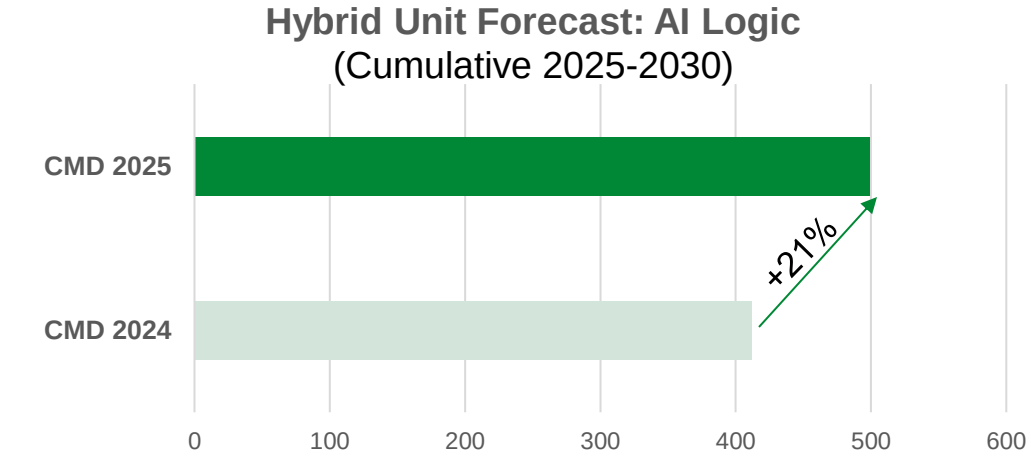
Google

BROADCOM

NVIDIA

amazon

GLOBAL FOUNDRIES



Hybrid Interconnect AI Use Cases are Solidifying

- Accelerated AI usage. Increased focus on energy efficient AI chips
- Hyperscalers like Meta and Google designing proprietary AI XPUs
- TSMC opening a new packaging factory for SOIC in 2026

Source: Besi estimates, June 2025

Application Drivers: High Bandwidth Memory

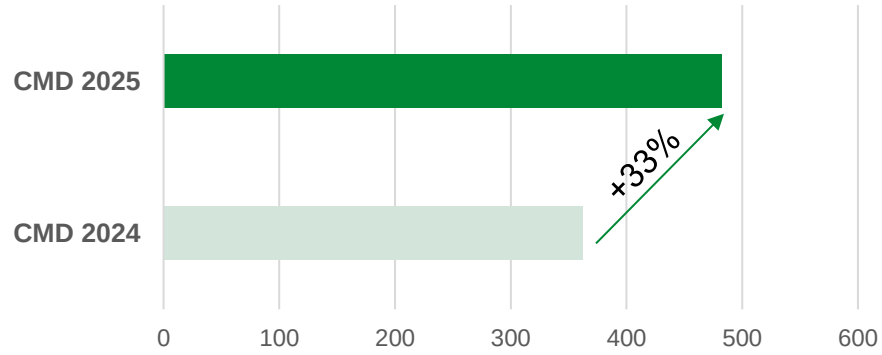
SK hynix

Micron

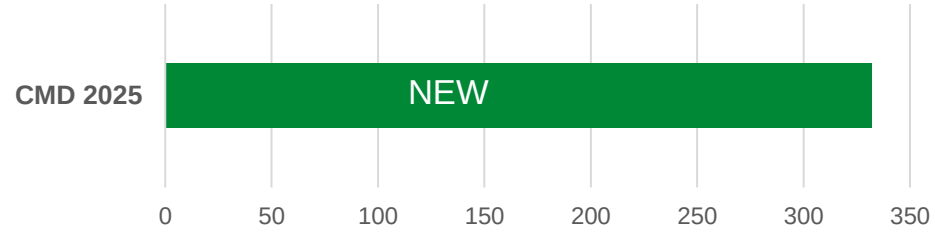
SAMSUNG

- Overall HBM demand is forecast to increase 4x 2025 - 2030
- TC and TC-fluxless will be primary technologies used through HBM4
- Hybrid bonding investments will start in 2026 accelerating in 2027/2028
- By 2030, majority of capex will be focused on hybrid stacking for 16+ high memory stacks
- TC ^{NEXT} investments in 2030 will be focused on replacing older TC technologies for medium-sized memory stacks

Hybrid Unit Forecast: HBM
(Cumulative 2025-2030)

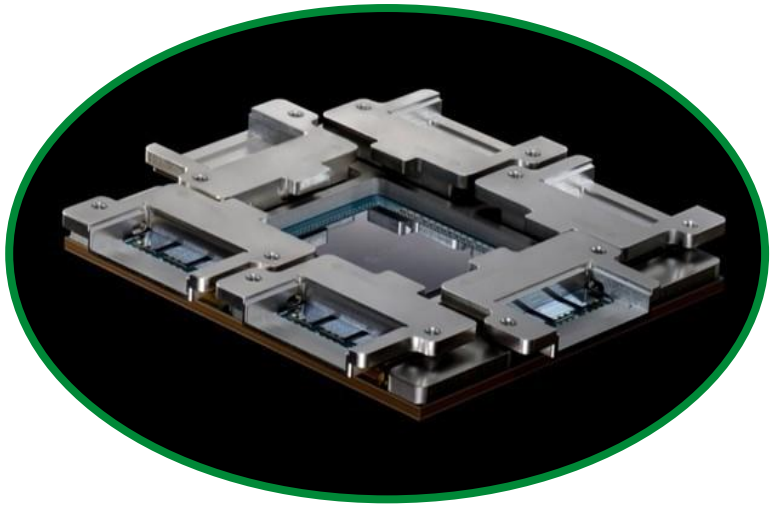


TC-Fluxless Unit Forecast: HBM
(Cumulative 2025-2030)

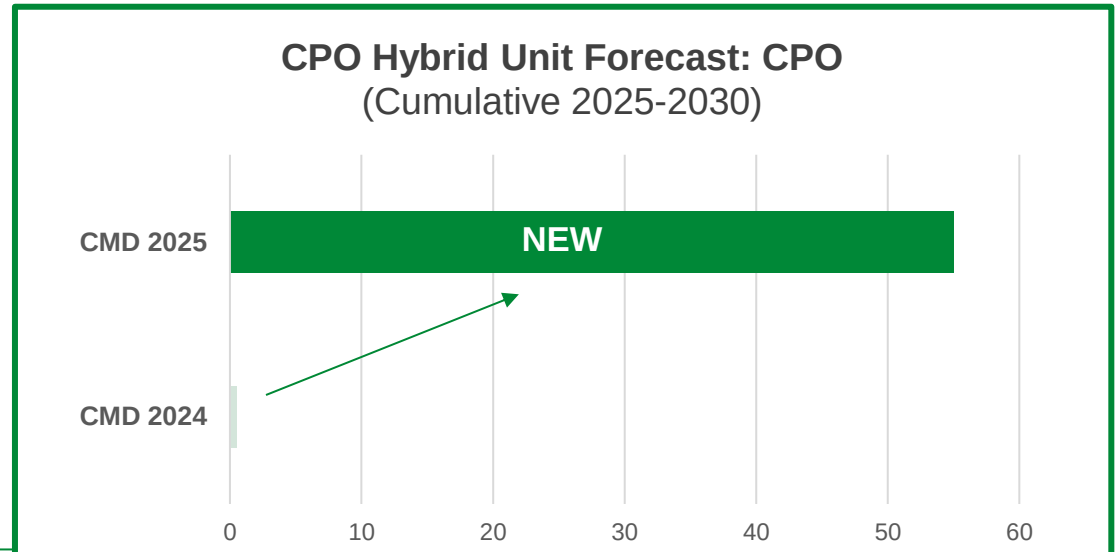


Source: Besi estimates, June 2025

Application Drivers: Co-Packaged Optics



- At GTC 2025, **NVIDIA** revealed use of CPO in their photonics network switches “Spectrum-X” and “Quantum-X”
- **Broadcom** announced its new Tomahawk 6 switch
  - *“For systems requiring optical connectivity, Tomahawk 6 will also be available with co-packaged optics, providing the lowest power and latency”*
- **TSMC** launched a CPO package called COUPE. Available for all photonics customers



Optical links now used to replace copper for short distance data transfer to connect individual boards within datacenters

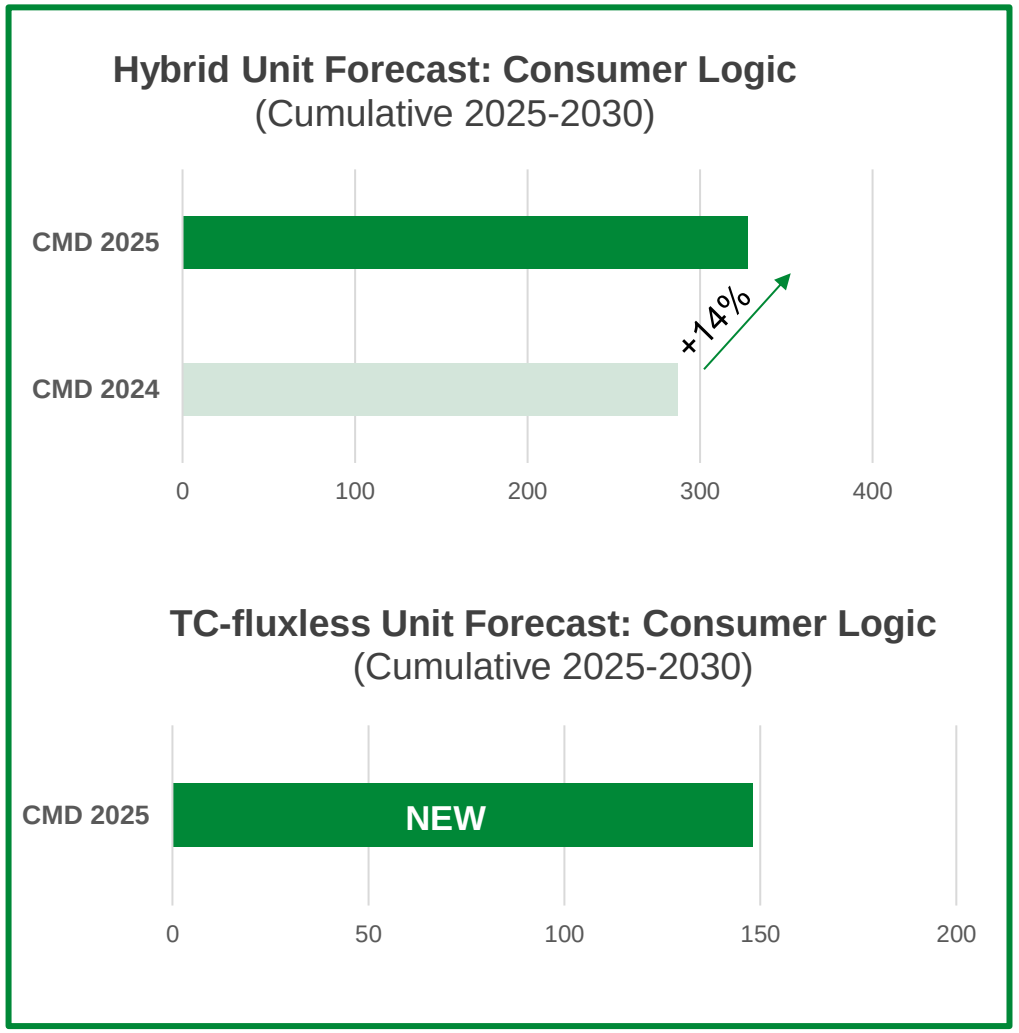
- Can achieve higher bandwidth at lower energy consumption (up to 80% savings)
- Hybrid technology being used in CPO to connect the photonic IC with the electrical IC @ high speed

Source: Besi estimates, June 2025

Application Drivers: Consumer: PCs - Tablets – Smartphones

AMD

- Adoption of edge AI driving need for energy-efficient performance beyond datacenters to also include consumer devices
- This will drive growth in both hybrid bonding and TC-fluxless
- Hybrid chiplet interconnect will be used for the most advanced edge-AI applications
- TC ^{NEXT} will cover the mid-range of application processors

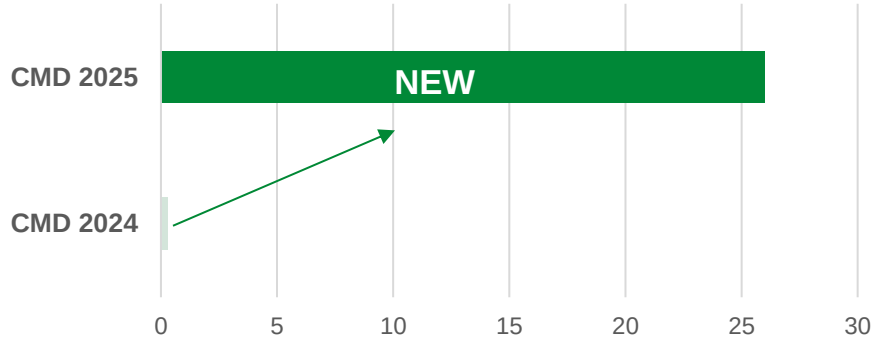


Source: Besi estimates, June 2025

Application Drivers: Consumer: AR Glasses – Optical Applications

Smart glasses prototype

Hybrid Unit Forecast: AR Glasses
(Cumulative 2025-2030)



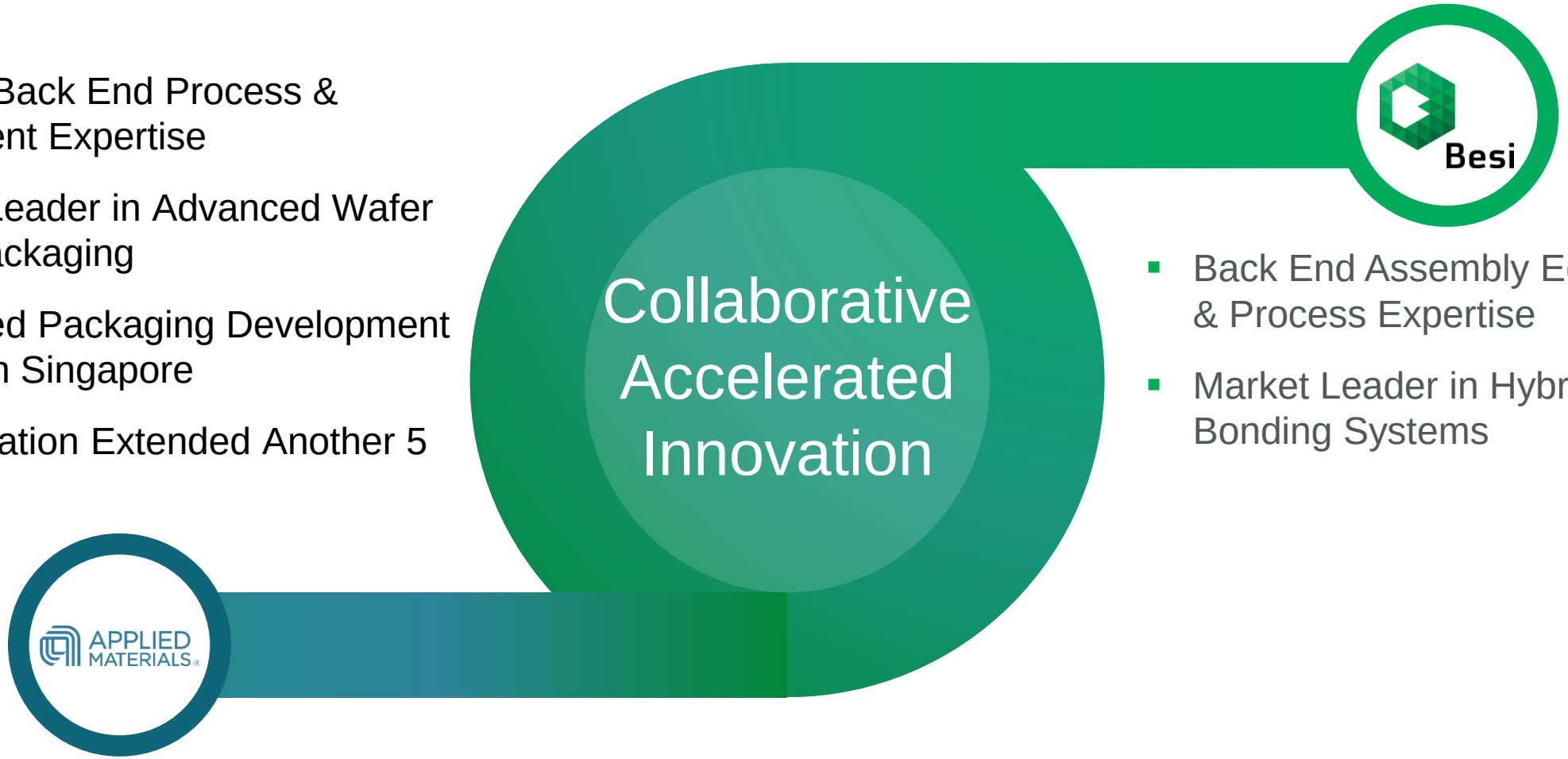
New application fields emerging:

- Advanced micro displays for smart glasses are using hybrid and fusion bonding technologies
  - Enables smart glasses comparable in size to conventional glasses

Source: Besi estimates, June 2025

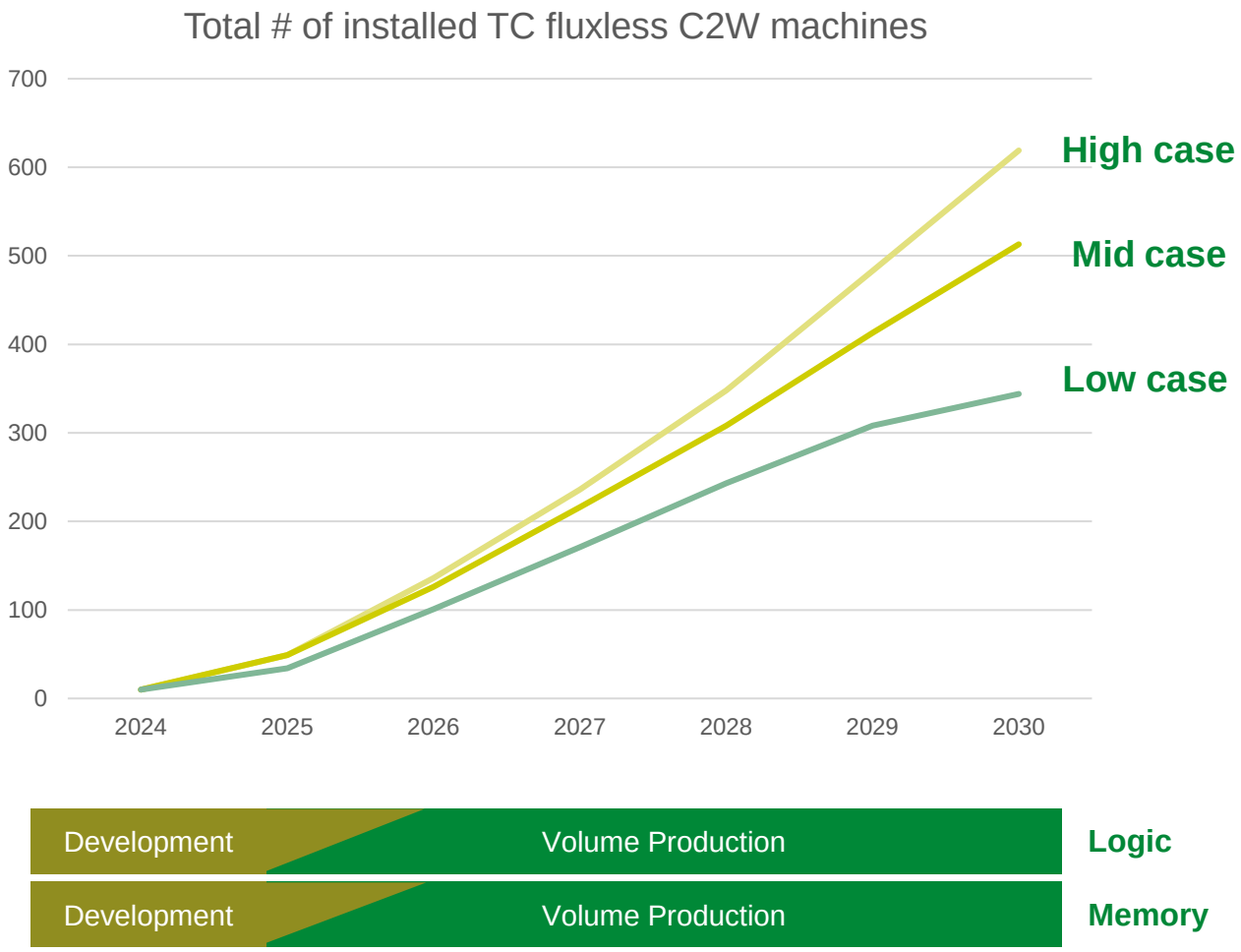
Applied Materials & Besi Collaboration Helps Accelerate Hybrid Bonding Adoption and Growth, 2 to 4 generations ahead

- Front & Back End Process & Equipment Expertise
- Market Leader in Advanced Wafer Level Packaging
- Dedicated Packaging Development Center in Singapore
- Collaboration Extended Another 5 years



- Back End Assembly Equipment & Process Expertise
- Market Leader in Hybrid Bonding Systems

Fluxless TCB C2W Market Potential



Source: Besi estimates, June 2025

Estimated 350 – 600 systems cumulatively by 2030

Fluxless TCB applications bridge gap between conventional TCB and hybrid bonding

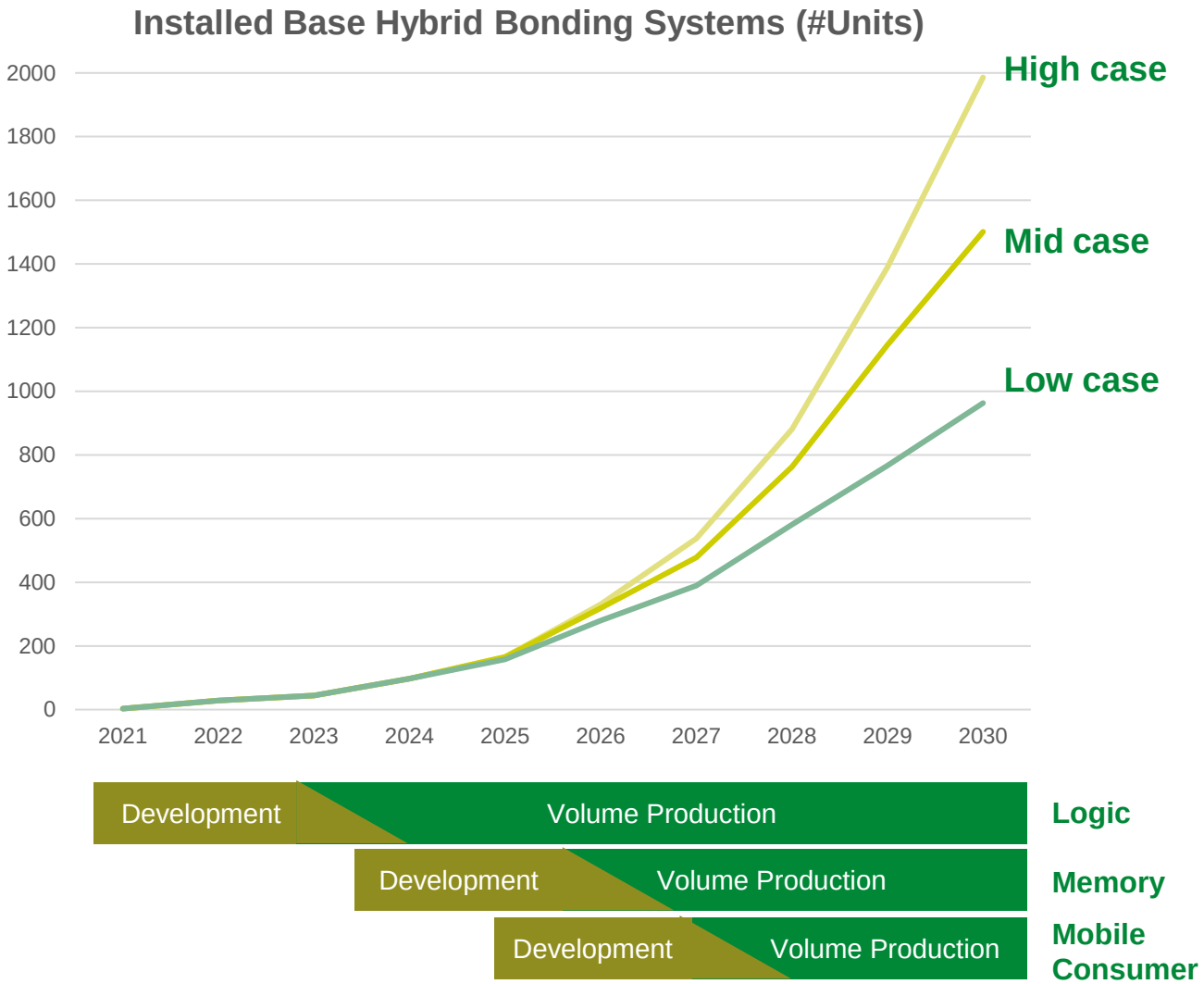
Memory:

- Next generation AI devices driving strong HBM demand in near term
- Increased HBM stacking requirements driving TC technology towards fluxless

Logic:

- Requirements for increased accuracy and chiplet architectures driving conversion of mid-end logic applications from mass reflow flip-chip to TC fluxless

Hybrid Bonding Market Potential – Logic and Memory Cases Confirmed



Source: Besi estimates, June 2025

Estimated 960 – 2,000 systems cumulatively by 2030
Up ~7% for low and mid cases vs. 2024 CMD

Low case (logic):

- Logic adoption confirmed
  - AMD and Intel progressing as expected
  - Broadcom adopting SoIC for custom AI ASICs
  - High-end PC/laptop CPUs expected to adopt SoIC by end of 2025
  - Many AI device players in development

Mid case (Memory & CPO):

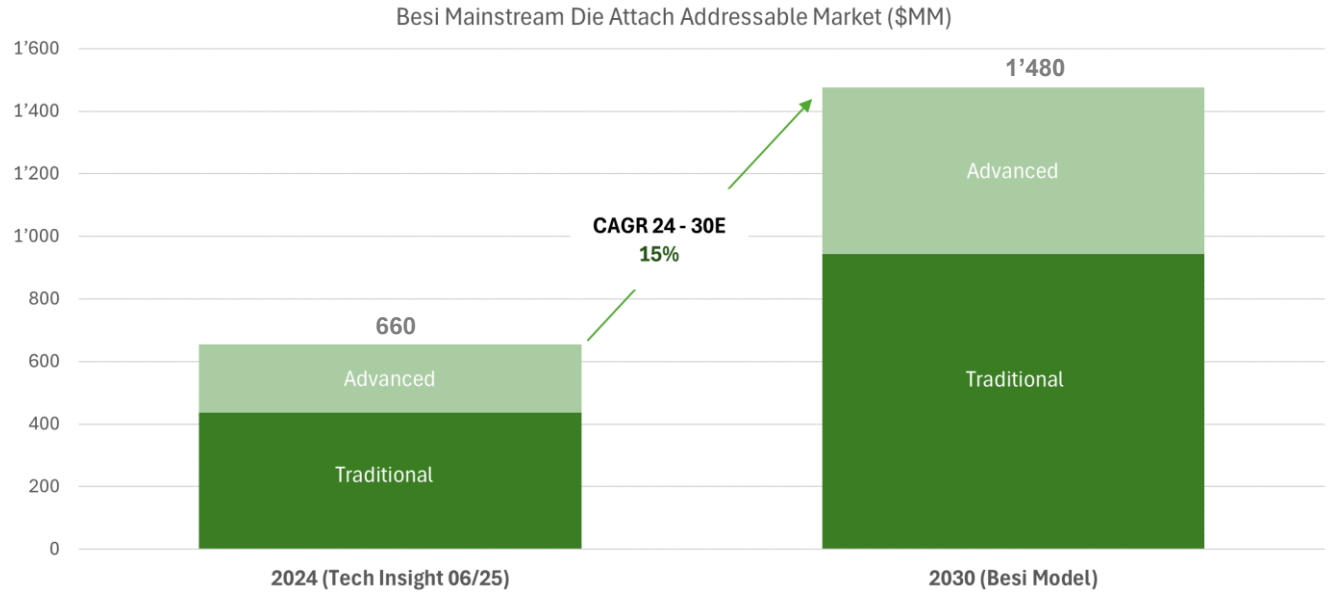
- Memory adoption confirmed
  - All leading players evaluating both HB and TCB for HBM4
  - First hybrid bonded HBM4e 16 high stacks in 2026
  - HBM 5: Hybrid bonding only
- Co-packed optics moves from upside potential to reality

High case:

- Emerging applications becoming more tangible
  - Smart glasses adopting D2W fusion bonding
  - Micro displays
  - Sensors
  - Smartphones

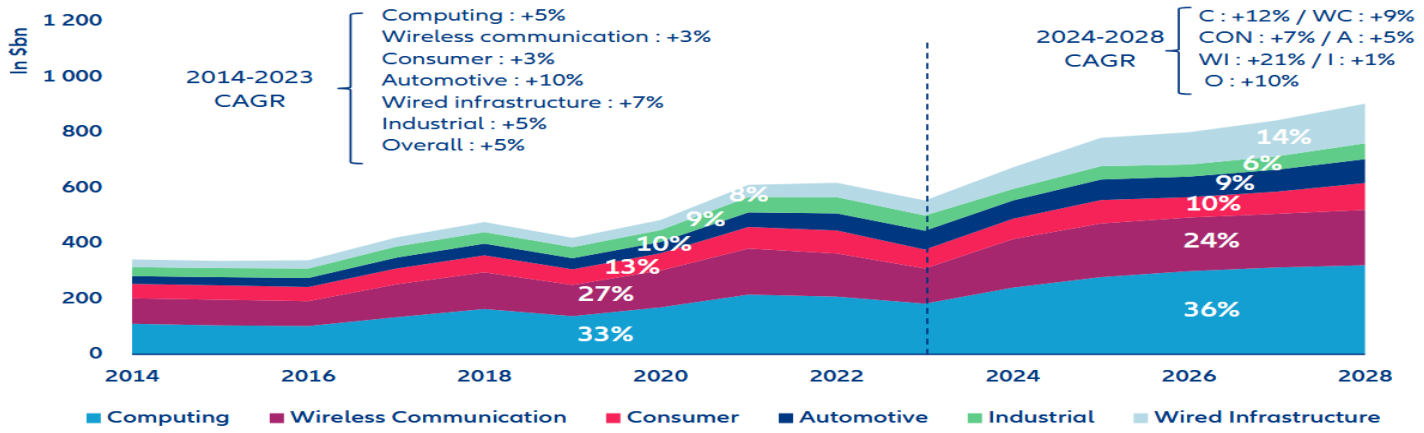
IV. MAINSTREAM DIE ATTACH
Christoph Scheiring
Senior VP Die Attach

Besi's Mainstream DA Addressable Market* Expected to More Than Double by 2030. Growth Anticipated Across All Product Lines



Source: Besi / Techinsights June 2025

Growth accelerating across all end user markets



Source: Allianz Research, 2025

Key Market Trends

- **Exponential growth in AI training workloads** drives data center expansion and demand for **HPC** and **Photonics**
- **Move to Inferencing** expected to drive next wave of equipment demand as applications deployed at scale
  - Increasing inference requirements will drive upside for mainstream **CPUs** and **ASICs**
- **Gen AI applications and edge AI demand** expected to drive mainstream consumer and industrial market
  - **PC, Mobile, IoT Sensors, Automotive**
- **Push for performance, efficient power and miniaturization** favors Besi's core advanced packaging solutions such as flip chip

* Excluding TCB, Hybrid, Die Sorting, LED

Industry Leading Mainstream Die Attach Equipment Portfolio with Significant Competitive Advantage

LG Innotek · intel · ST life.augmented · Infineon · INNOLIGHT Innovation Lights Our Future · BOSCH · NVIDIA · FOXCONN SHARP · fabrinet

- Highest accuracy for photonics and CPO
- Leading process capabilities for large die AI interposer attach and advanced camera modules

Multi-module

Flip Chip

ASE GROUP · BESI · JCET STATSChipPAC · PTI · HUA TIAN · Amkor Technology · TF · unisem · SJSEMI

- Highest accuracy C2W (2.5D CoWoS) assembly
- Highly productive tool of reference in BGA & CSP & LF flip chip attach
- New tailored high speed solution for camera modules

Soft Solder

Infineon · ASE GROUP · ST · HUA TIAN · TF 通富微電

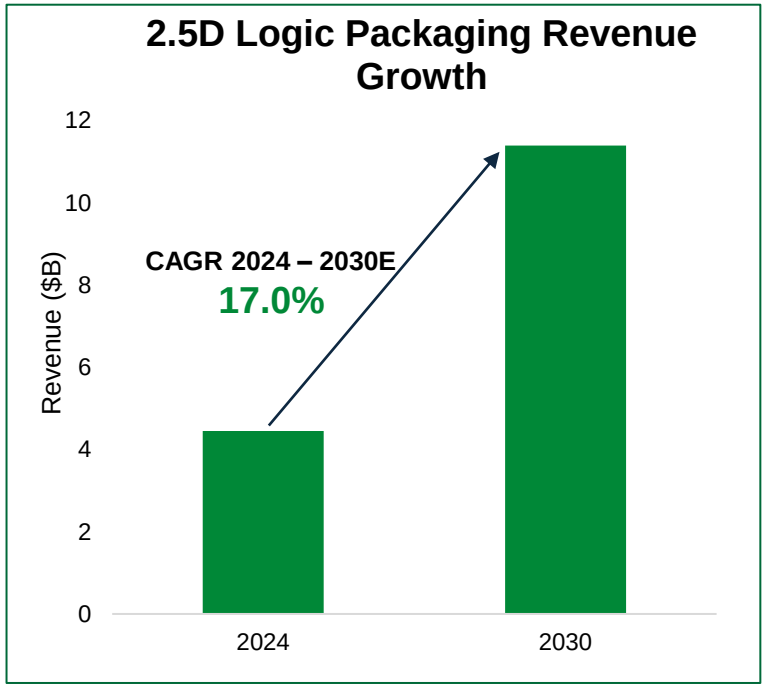
- Leading soft solder process (oxygen level, gas consumption) for automotive power applications
- Unique diffusion solder process offering

Epoxy

HUA TIAN · NXP freescale · Infineon · UTAC · GREATEK ELECTRONICS INC. · TF · Carsem · JCET STATSChipPAC · ASE · Amkor Technology · qorvo

- Industry leading accuracy and speed in epoxy die attach
- Stringent epoxy control for mobile and automotive power and sensor applications

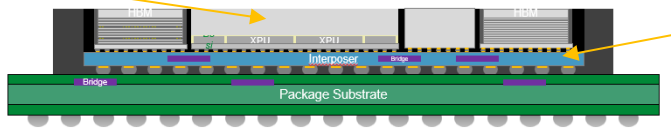
Portfolio Well Positioned in High Growth 2.5D Advanced Packaging



Source: Yole, High End Performance Packaging 2025

2.5D package architectures require new flip-chip capabilities to support multiple chiplets including higher accuracy, higher productivity and greater flexibility

High Speed CoW (Logic & HBM)



8800 Chameo advanced / TnR

- Placement accuracy 3um
- High speed flip chip attach
- Inline wafer and tape and reel configuration

Large Die Interposer Attach

2200 Evo advanced

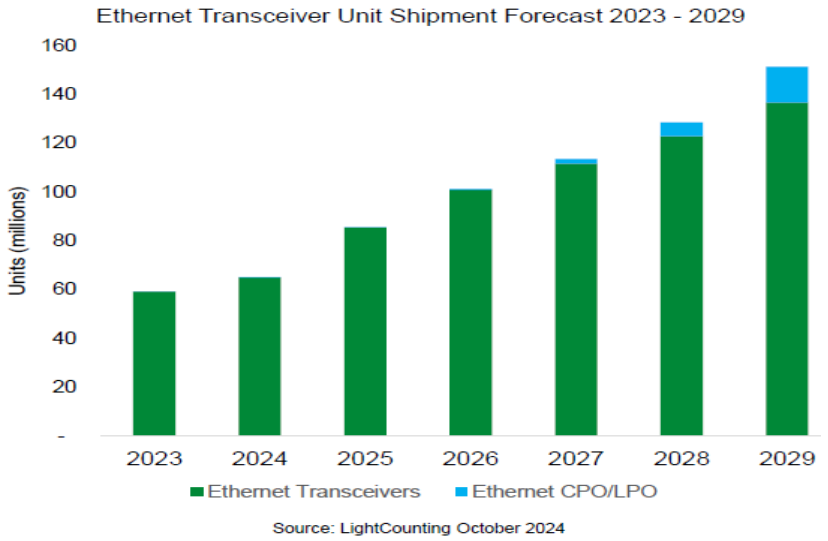
- Large die flip chip
- 110mm x 110mm
- OHT integration

NEW 8800 Chameo *Flex* (2026)

- Highest productivity/integrated CoW solution
- Placement accuracy 1um
- Full front-end automation

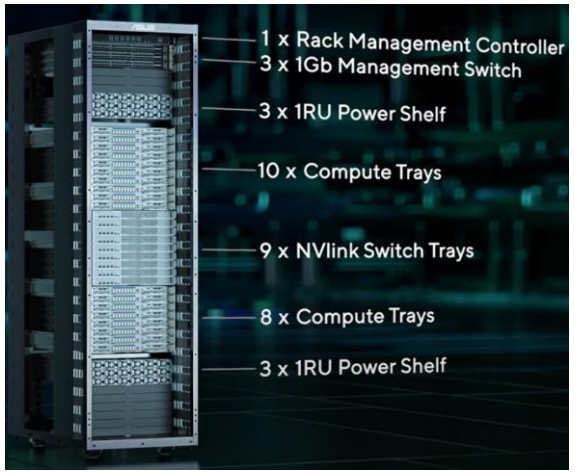
Besi's Multi Module Attach System: Leading Photonics Platform in Rapidly Growing Market

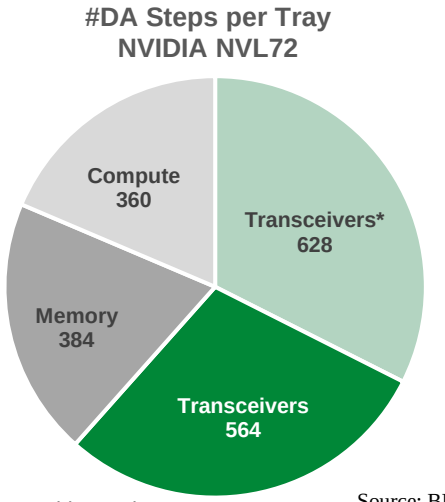
Data center expansion driving demand for optical connections



Optical transceivers in today's AI servers require a significant number of die attach steps

NVIDIA NVL72



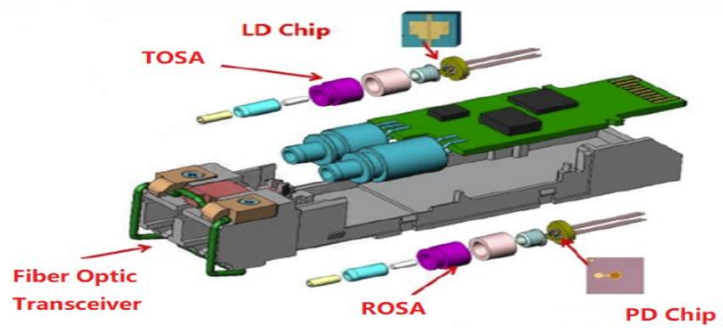


* Currently not addressed

Source: BESI

Besi # 1 player in optical transceiver assembly working with all key players

Typical Optical Transceiver Assembly



Source: Nvidia

NVIDIA · INNOLIGHT · COHERENT · fabrinet · molex · eoptolink · FINISAR · Accelink · HG Semiconductor Limited 宏光半導體有限公司

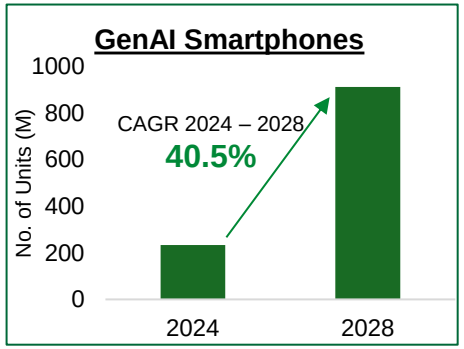
2200 Evo advanced

- Best combination of placement accuracy and productivity
- Versatility in complex system assembly
- Ultimate process control
- Significant installed base with industry leaders

NEW Evo 1um (2026)

Introducing new 1um accuracy system (replacing active alignment) to increase optical transceiver market share

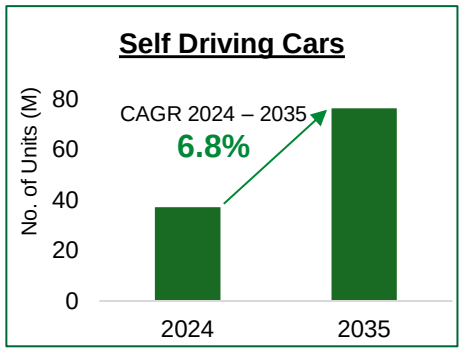
Edge AI Drives Semiconductor Market Recovery and Demand for Besi Mainstream Die Attach Equipment



Source: IDC July 2024

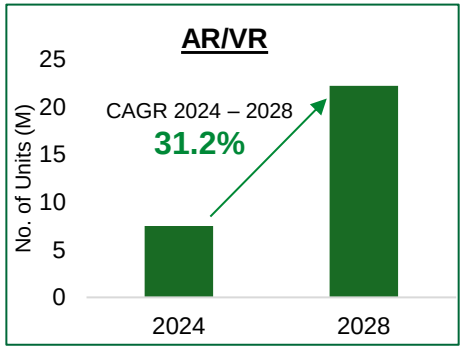
- AI drives high-end smartphone segment with richer content (AP, memory, camera)
- New camera applications in pipeline (mechanical aperture, stacked lens assemblies)

Source: Cambridge Mechatronics



Source: MarketsandMarkets Dec 2024

- AI gaining traction in automotive sector (from driver assisted systems to autonomous vehicles)
- Advanced packaging enabled electronic content in cars is increasing



Source: IDC Dec 2024

- AI in combination with AR/VR is changing how people interact with the digital world
- AR/VR HW requires new forms of miniaturized, energy efficient, high-performance packaging

Besi Mainstream die attach solutions are preferred choice for AI driven advanced packaging needs

2200 evo

Application Drivers

- Smartphone camera
- Automotive and industrial power modules
- AR/VR devices

2100 hSi / SSI / FC

Application Drivers

- Mobile RF power amplifiers
- Mobile sensors
- Power management ICs

8800 FCQ / Chameo / CIS

Application Drivers

- Processors (Mobile AP, GPU, CPU, ASIC)
- DRAM

NEW 8800 CIS

- Introduction of high-speed platform for advanced camera module assembly

Summary

- **AI driving customer investments** in next generation devices and applications requiring advanced packaging
- Besi's mainstream die bonding **addressable market expected to more than double** by 2030
- **Favorably positioned** in highest growth segments of advanced packaging:
  - CoWoS
  - Photonics
  - Mobile
  - EV/autonomous driving
- **New product introductions in 2025-2026** expected to accelerate growth and increase market share

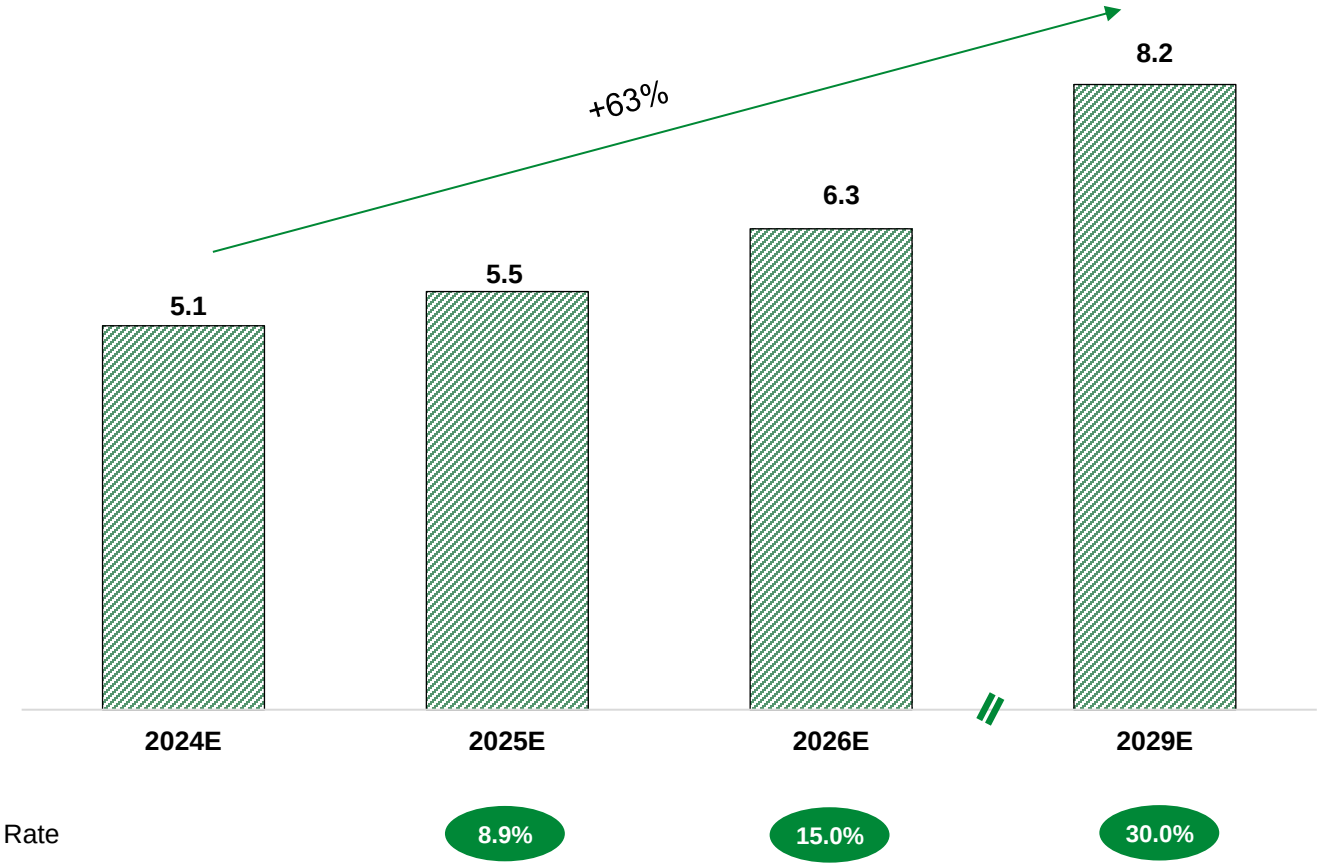
V. STRATEGIC PLAN UPDATE
Richard Blickman
CEO

Strategic Plan Updated to Position Besi for Advanced Packaging Growth 2025-2030

Strategic Plan Update 2025

- **16-week process**
  - Senior management, customers and other key stakeholders involved
- **Revenue and cost reduction goals established**
- **Multiple secular growth drivers identified**:
  - Expanded AI deployment and use cases across principal end user markets
  - Increased chiplet adoption for heterogeneous integration
  - Increased HB and TCB Next adoption for <3 nm node sizes
  - Increased investment in advanced packaging fabs
- **Capacity, personnel planned to meet growth expectations**

Long-Term Market Opportunity



Long-term growth trends intact:
- Expansion of AI/use cases
- Advanced packaging growth in all end-user markets

Significant assembly growth forecast between 2024-2029
- 25% increase anticipated 2024-2026
  - AI and cyclical mainstream recovery
- 63% increase expected 2024-2029

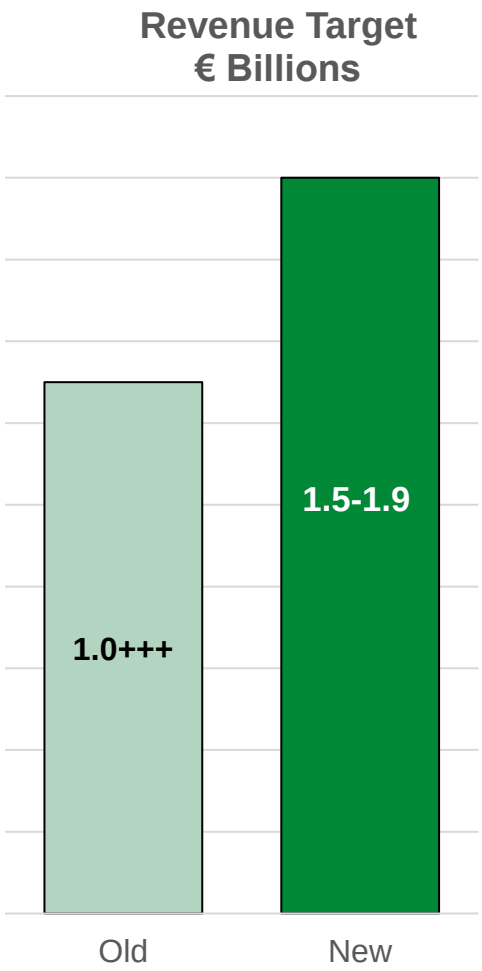
Besi expects to significantly outperform overall growth rate for assembly equipment market

Source: TechInsights, June 2025. Assembly equipment revenue excludes service revenue

Target Model Update

Prior Long Term Target		New Long Term Target
€ 1 billion +++	Revenue	€ 1.5-1.9 billion
40%+	Addressable Market Share	40%+
62-66%	Gross Margin	64-68%
35-50%	Operating Margin	40-55%
Net Zero GHG by 2030	Scope 1 & 2 Emissions	Net Zero GHG by 2030
100% from renewable sources	Global Energy Needs	100% from renewable sources

Key Revenue Growth Drivers



Hybrid Bonding

- Expanded logic adoption as new use cases emerge
  - Heterogeneous chiplet integration, datacenter, Edge AI, CPO
- Expanded consumer applications for mobile, PCs, wearables, AR/VR
- Memory adoption for HBM 4/5
- Increased market penetration via Applied Materials integrated production lines

TCB Next

- Transition from Chip to Substrate to Chip to Wafer at leading edge
- Expanded use in HBM 4 and advanced CoWoS applications
- Significant upside market share potential

Advanced 2.5D / Mainstream

- Increased penetration of photonics, smart phone, power module and mobile memory markets with next gen multi module and flip chip systems
- New mobile innovation: advanced cameras, sensors, AP packaging and phone form factor
- Packaging: Chiplet molding and singulation, SiC and GaN power device molding
- EV and autonomous driving

Spares/Service growth scales with expansion of sub-micron die attach installed base

Key Operational Goals

Gross Margin

- Target € 15-30 million cost reduction
  - Realize further design efficiencies via common parts/platforms/modules

Operating Expenses

- Investment in R&D and Service/Support to support sub-micron die attach growth
- Limit G&A growth to rate of inflation

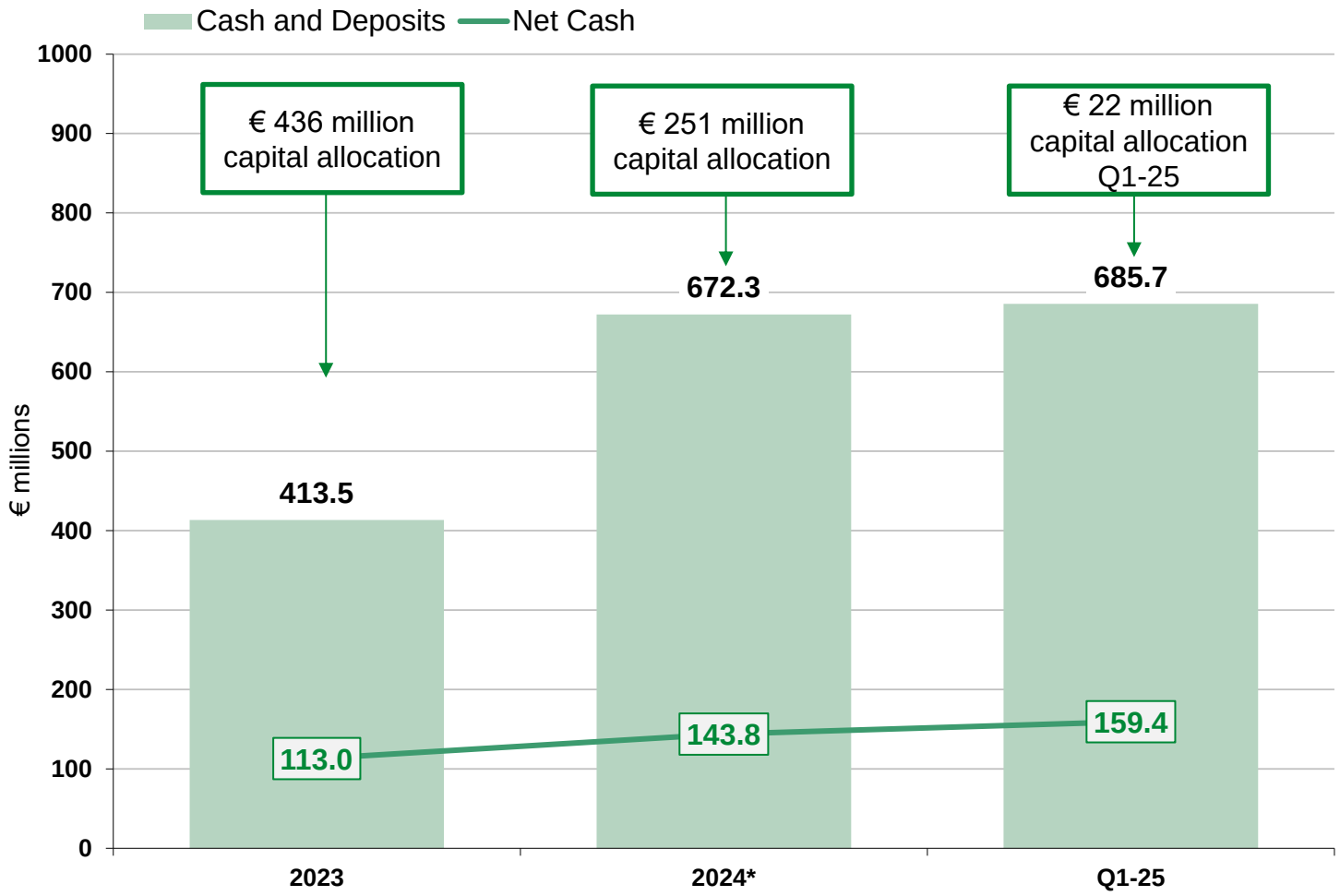
Operations

- Expand presence in SE Asia and India per customer roadmaps
- Increase cleanroom capabilities

Sustainability

- Net zero GhG emissions by 2030
- 100% global energy needs from renewable sources

Strong Liquidity Position for Future Growth
Attractive Capital Allocation Policy Continues



Shareholder friendly capital allocation

- € 2.2 billion distributions since 2011*
  - Equal to ~33% of cumulative revenue
- € 22.1 million distributed YTD Q1-25
- € 51.4 million purchased under current € 100 million share repurchase program
- Treasury shares equal 2.0% of TSO

Attractive funding to help finance growth:

- € 197.7 million Convertible Notes
  - Blended interest rate 1.74%
- € 350 million 4.5% Senior Notes due 2031
- € 80 million revolving credit expandable to € 136 million

* Includes dividend paid in May 2025

Summary

Assembly Market at Major Growth Inflection Point

- AI expansion drives continued advanced packaging adoption
- Slowing of Moore's law accelerating adoption of chiplets and 3D IC

Besi Developing Complete Portfolio of Complex Chip Packages For World's Leading Semiconductor Producers

- New system introductions planned in 2026 for CoWoS market

Hybrid Bonding Technology of Choice for High Performance, Energy Efficient Computing

- Hybrid bonding and TC Next anticipated to be fastest growing assembly segments over next 5 years
- New use cases emerging in logic, CPO, memory and consumer applications
- Hybrid bonding market potential increased 7% versus 2024 CMD

Strategic Plan Updated to Position Besi for Advanced Packaging Growth 2025-2030

- Long-term revenue, gross margin and operating margins increased reflecting incremental upside potential

Attractive Capital Allocation Policy Maintained

VI. Q&A

Investment Considerations

Besi

- Assembly market ever more critical in semiconductor value chain
- Disciplined strategic focus has created an industry leader
- Long term secular trends drive advanced packaging growth
- Wafer level assembly for AI applications promising new growth opportunity
- Market presence has grown via key IDMs, supply chains and partners
- Tech leadership and scalability result in superior financial returns
- Commitment to sustainable growth and fighting climate change
- Attractive capital allocation policy