Die-to-wafer hybrid bonding development for HVM

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This article addresses the key requirements for a successful die-to-wafer (D2W) hybrid bonding process. The selected process steps from bonding pad formation to grind and singulation, as well as an integrated D2W bonding process will be addressed, providing key technical values for the various steps involved. The integrated bonding processes include wet cleaning, degassing and plasma surface treatment. Successful Cu-Cu diffusion through grain growth across the boundary interface will show the efficacy of such a tool, C-mode scanning acoustic microscopy (C-SAM) results will address the topic of voids, and electrical yield results will also be presented. Actual placement accuracy results will also be shared for both collective and direct D2W hybrid bonding.

Introduction

The adoption of 3D architectures in advanced packaging between chips is driven by high-performance computing (HPC) and artificial intelligence (AI) requirements [1, 2]. Flip chip has been the main technology of forming the die attachment in packaging. It requires a copper (Cu) pillar made out of a metal alloy, namely copper-nickel-tin-silver (Cu-Ni-Sn-Ag) that occupies an opening with a critical dimension (CD) of 20-40µm on a passivation polymer dielectric (e.g., polymide or polybenzoxazole [PBO]) for each of the contact points. Such a thickness is needed to allow underfill material to flow reliably and to act as a stress buffer for mechanical integrity. The flip-chip attach is done through thermal compression bonding (TCB) where at least one of the dies or substrates is heated to ensure that the Cu bump reaches the eutectic state so that Sn-Ag can form a good electrical contact. With this bonding technique, some amount of inter-metallic compound that is causing higher resistivity and weaker reliability is inevitably generated.

The migration toward Cu hybrid bonding (HB) will only require the use of standard back end of line (BEOL) inorganic dielectric and Cu, and is expected to improve over the issues noted above, as well as adding other benefits. Overall, the preparation needs for die bonding are simplified, Cu bump and underfill processes are removed, and TCB is replaced with room temperature HB. This directly translates into reduction of vertical form factor and scaling to higher input/output (I/O) density, thereby leveraging the mature BEOL that scaled well below the sub-micron range. The change of pad material from a complex alloy (Cu-Ni-Sn-Ag) to pure Cu and the direct connection through HB at room temperature are expected to offer shorter interconnect lengths, lower resistance and improvement in thermal diffusion. As a result, an increase in system-level performance with better bandwidth and/or speed can be expected.

HB is achieved as a two-step process: first, by leveraging on the initial forces of surface interaction at atomic proximity of the dielectric-dielectric interface to form the "tacking," which is the initiation of the bonding, and finally, following up with a fusion process by annealing at an elevated temperature (100°C-400°C) to form both stronger dielectric-dielectric covalent bonds with the release of excessive water (H_2O) molecules, as well as metal-metal diffusion that will enable the electrical connection. A successful bond can be achieved with careful surface engineering of the dielectric, typically with dielectric surface roughness values of <0.4nm [3]. Of the two HB flavors, wafer-to-wafer (W2W) or D2W, the latter enables higher system-level yield thanks to use of known-good-dies only. This paper describes the necessary conditions to achieve a successful D2W HB suitable for high-volume manufacturing (HVM) production.

PVD-CMP co-optimization for D2W HB

As elegant as it looks, HB also has many challenges. The bonding requirements that work for W2W HB, e.g., the Cu chemical mechanical polishing (CMP) process that ensures good roughness (<0.4nm), dishing (<5nm) and erosion, are not directly transferable to D2W. A D2W test vehicle and bonding flow was developed based on the illustration of the key process sequence shown in **Figure 1**. Previous work done on W2W test vehicles successfully demonstrated thick barrier and

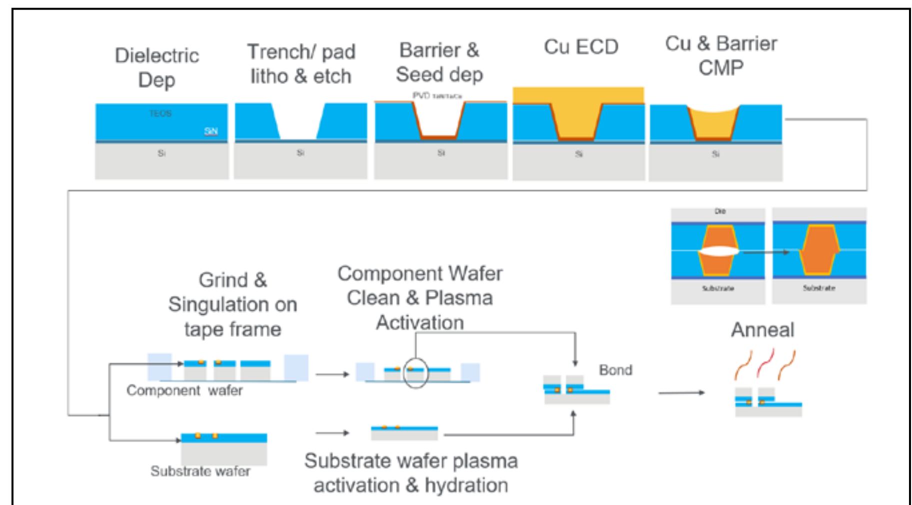

Figure 1: Selected process steps from bonding pad formation to grind and singulation.

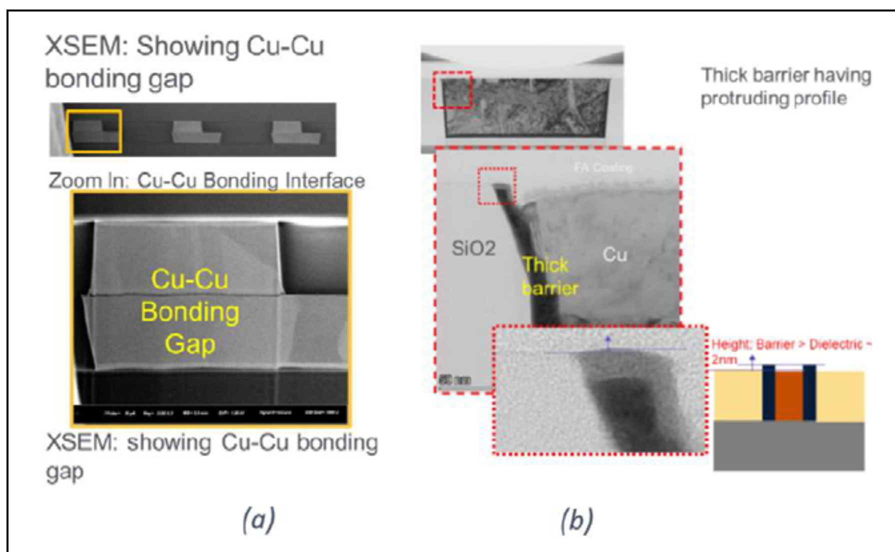

Figure 2: a) A PVD thick barrier-CMP interaction with zoom in focus and an illustration of barrier protrusion, which resulted in b) a Cu-Cu bonding gap due to barrier-CMP interaction (see the XSEM).

CMP optimization [4]. However, when the same process was applied to D2W HB, it resulted in a visible Cu-Cu gap from X-ray secondary emission microscopy (XSEM) analysis as shown in **Figure 2a** due to insufficient force (weight) to form good tacking (i.e., low force was used to bond the samples compared to the forces used in W2W bonding) as a result of thinning and dice. The failure analysis of a cross section with transmission electron microscopy (TEM) at the edge of the Cu bond pad (**Figure 2b**), indicated the barrier was higher than the dielectric by 1-2nm. One hypothesis suggested that this barrier protrusion was standing out from the rest of the dielectric at the corner of the bonding pads, and in addition to the already reduced force acting on the bond interfaces from grinded and singulated die, was preventing the "tacking" of dielectric-dielectric during die placement. At post-bond anneal, the protruded barrier has higher thermal expansion than the oxide (Ta: 6.5 10^{-6}/K vs. SiO_2: 0.65 10^{-6}/K [5]) and therefore was expanding faster, pushing the two bond interfaces apart and preventing the Cu pads from making contact and diffusing (or inter-diffusing), giving rise to a wider gap (20~40nm) than initial dishing. The physical vapor deposition (PVD) barrier-CMP process was optimized by using a thin barrier and a tuned CMP process to ensure that oxide was always higher than the barrier as shown in **Figure 3a**, while keeping the roughness, Cu dishing and erosion within the D2W bonding process requirements. The same bonding and annealing was repeated. The results showed that the Cu-Cu bond was fused, and was further validated with transmission electron-back-scatter-diffraction (T-EBSD) portraying a successful Cu diffusion across the bonding boundary (**Figure 3b**).

Surface activation, cleanliness, queue time and electrical yield

Once the interfaces were optimized as discussed in the section on PVD-CMP co-optimization, we moved on to study dielectric surface activation, the impact of a particle-free surface and queue time. These requirements are more stringent for D2W HB than for W2W HB because of the need to process dicing and singulated dies on flexible organic tape or on carrier wafers with organic adhesive.

Plasma activation has been demonstrated to increase hydrophilicity for dielectrics such as SiO_2 and SiCN [6]. Hydrophilicity is achieved by the presence of the silanol groups (Si-O-H) on the dielectric surfaces. Ion energy is one way to promote the silanol groups' attachment to the dielectric surface by creating disorders and high-energy states on the surfaces. The presence of these silanol groups is essential, as they enable initial bonding when dielectric surfaces from substrates and chiplets are brought together even at room temperature. The measurement of the hydrophilicity of dielectric surfaces is a way to evaluate the effectiveness of the activation

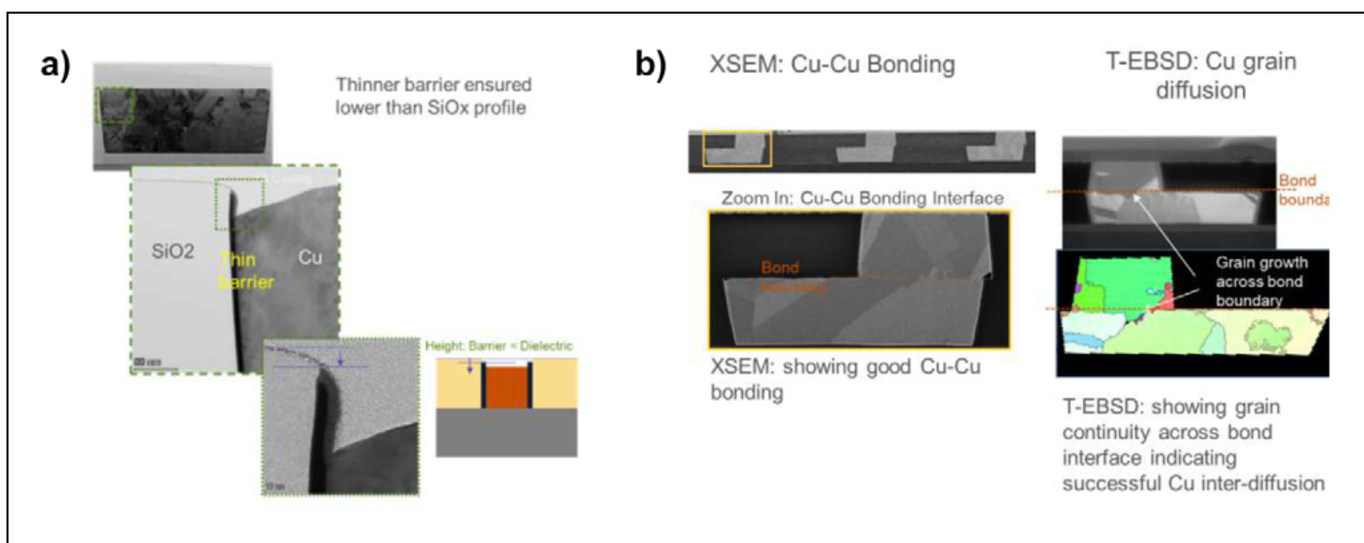

Figure 3: a) An optimized thin PVD-CMP, with zoom in focus and an illustration of higher dielectric than barrier in nm-scale, which resulted in a Cu-Cu diffusion (see the XSEM) and confirmation with T-EBSD showing grain growth across the bond boundary.

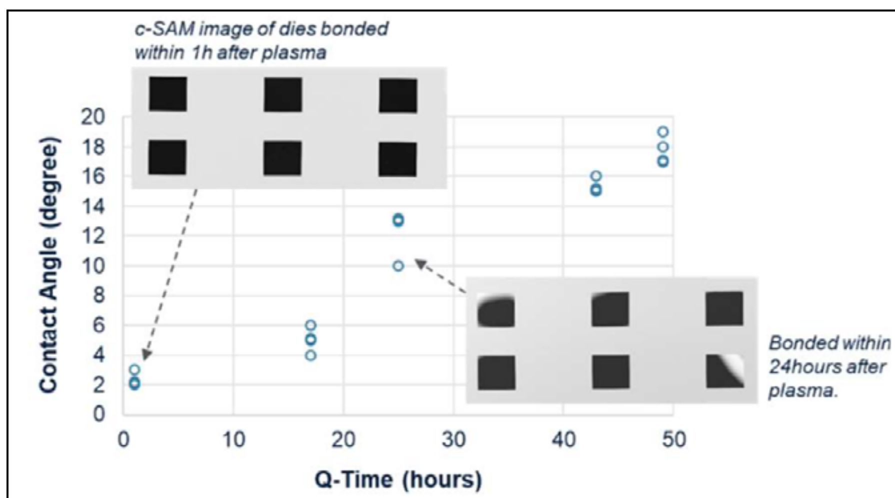

Figure 4: Plot showing the plasma activation effect on the initial contact angle on an SiO_2 surface and the queue time effect on the contact angle and bonding performance after activation. Bonding degrades with excessive queue time between activation and bonding as shown in the C-SAM images of the delamination around the die edges.

process. Macroscopic observations of the hydrophilicity of the SiO_2 surface are seen with water contact angle measurements. When the SiO_2 dielectric surfaces are treated with the right plasma conditions, superhydrophilicity with a contact angle of <5° can be achieved (**Figure 4**). It is also shown that the contact angle degrades over time if the wafers are exposed to air after activation. The degradation or the hydrophilicity leads to poor bonding performance, as shown in delamination at the die edges from C-SAM analysis (see insets of **Figure 4**). Therefore, controlling the queue time between activation and bonding is crucial to achieving the best bonding performance.

Proper selection of plasma conditions, including ion energy, density, and chemistry is essential for sufficient activation without causing physical or chemical damage to other materials, such as Cu and plastic tapes. As shown in **Figure 5**, when the ion energy is too high, the dielectric surfaces are roughened, which creates voids and diminishes the bonding performance. In addition, the sputtered materials from the dielectric surface and organic adhesive can further redeposit on the die surface under strong plasma conditions. The redeposition creates an undesired Cu diffusion barrier during the post-bonding annealing stage. Therefore, it is important to optimize the plasma activation conditions to achieve surface roughness of <0.5nm and etching of SiO_2 of <1nm while preserving the Cu dishing profile and ensuring the surface is free of organic residue and without excessive oxidation (**Figure 5e-h**).

Cleanliness is paramount to the performance of the HB. Any particle on the bonding surface can lead to poor adhesion, weak bonds, or complete failure of the bond (**Figure 6**). To ensure the best bonding performance, free particle control is a high priority for any pre-treatment system design. Particles should be controlled to meet the device specification in the activation chambers. In addition, a highly efficient wet clean process is essential to ensure the cleanliness before the wafer and the component dies enter the bonders. Efficient cleaning is particularly challenging for diced wafers on flexible tapes because the dicing processes could introduce additional particles or/and contaminants. Insufficient post-dicing cleaning could leave particles on the tape or die sidewalls (**Figure 7a-b**). In some cases, further cleaning, if not done correctly, can create more particles when stirred up from the tape or die sidewalls and land on die surfaces, causing delamination near die edges (**Figure 7c-f**).

After the whole integration, bonding process optimization and alignment were done, a 300mm substrate wafer was bonded (~230 dies) to validate the bonding performance. **Figure 8a** shows the post-bond C-mode scanning electron microscopy (C-SAM) result where no gross random void was observed, indicating high cleanliness efficiency. This is further confirmed with an electrical continuity test on a 10,000-daisy chain (DC) connectivity occupying an area of 1mm x 1mm (of a 6mm x 6mm die size) shown in the **Figure 8b** wafer contour plot and in the

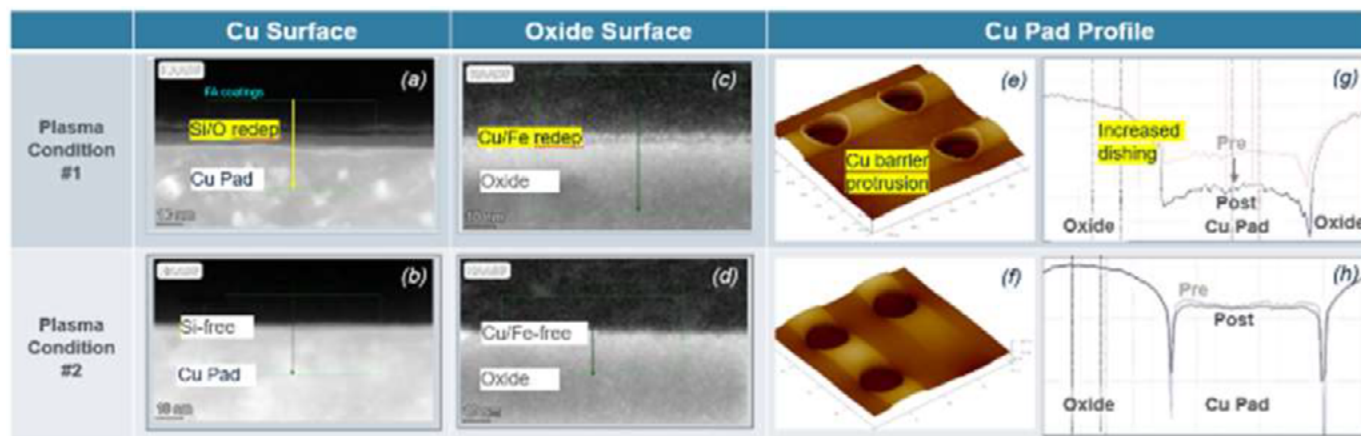

Figure 5: Surface and topography comparison between strong and soft plasma-treated patterned samples: a–d) TEM cross-sectional study of the Cu pad and dielectric oxide surface, revealing surface contamination from redeposition caused by a strong plasma; e–h) Atomic force microscope measurements showing that a strong plasma alters Cu pad profile, and an increased dishing amount.

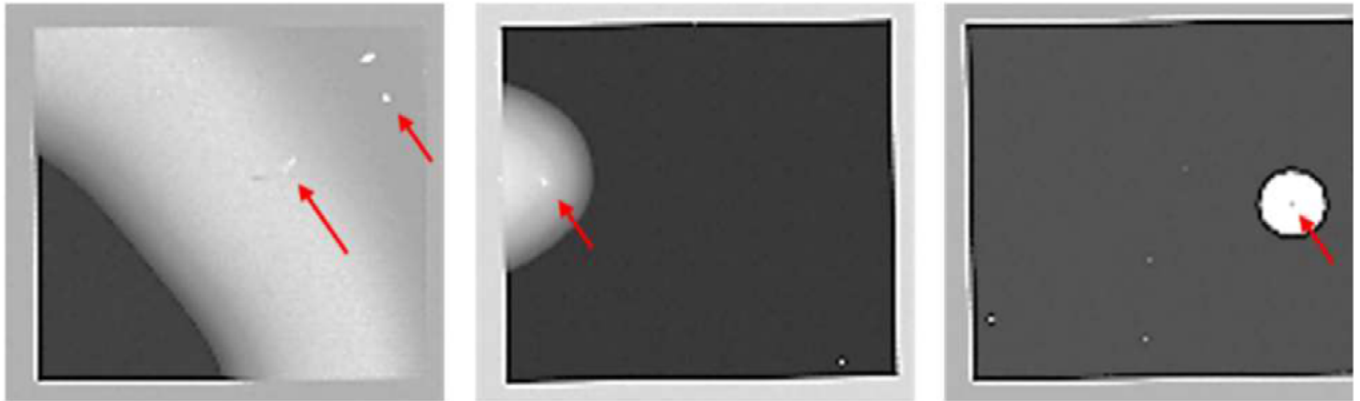

Figure 6: SAM images of defective bonding (delamination and voiding) caused by surface particles.

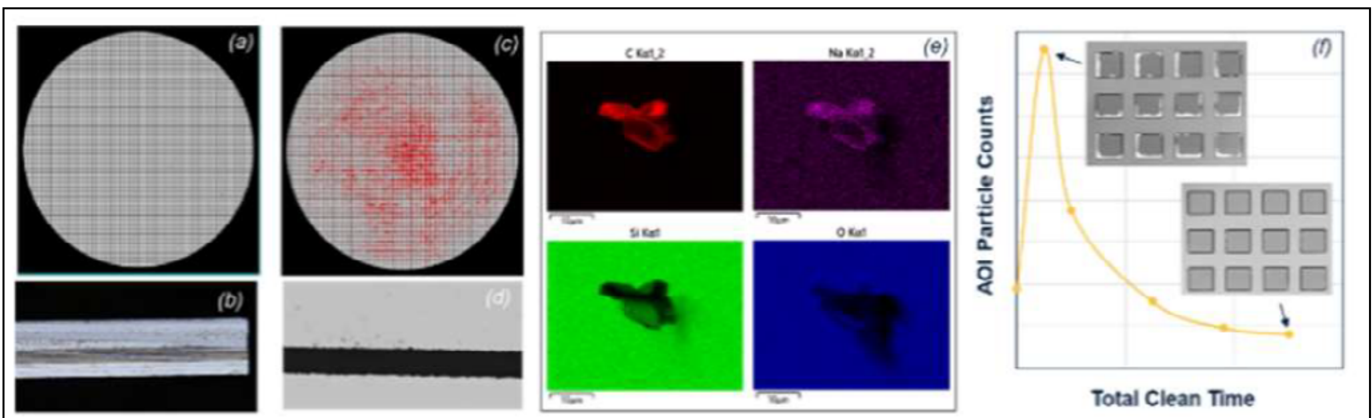

Figure 7: Automatic optical inspection (AOI) of the a) surface and b) sidewall of singulated dies of a tape-frame wafer after thinning and the saw-dicing process. A large number of particles (black) can be seen adhering to the sidewall. c-d) An incorrect further cleaning detaches and redeposits the particles onto the die surface. c-e) The organic nature of the particles revealed by energy-dispersive X-ray spectroscopy inspection suggests tape adhesive as the origin. If not properly removed, f) these particles can cause die delamination after bonding, as seen under SAM inspection.

normal quantile plot in **Figure 8c**, which shows a >99.5% continuity electrical test yield (a significant improvement from pre-optimization data). The process improvement was reflected in overall mean resistance and variability.

The same test vehicle was further used to characterize the process-induced possible yield impact of queue time between the various process steps, as batch-mode processing makes it difficult to control queue time. Samples were processed with a 36-hour queue time and compared with the baseline; in the high-volume production case, one could expect a queue time of 1 to 2 days, and not just time, but also its variance increases with a more complex bonding configuration, where >3-5 different chiplets are in the roadmap to be bonded to the same substrate. Three bonded wafers from the "delayed" lot were compared to the baseline in **Figure 9**. Adding queue time leads to significantly lower yield (80%) vs. the reference case (98%).

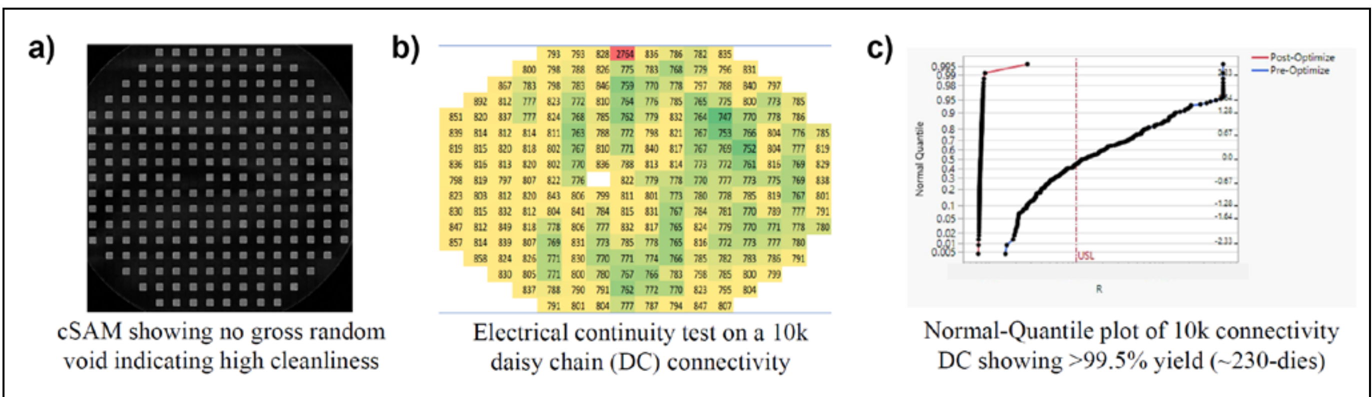

Figure 8: Post optimization: a) CSAM result showing void-free bonding, b) a wafer contour plot of 10,000-connectivity daisy-chains resistance, and c) Normal-quantile plot of 10,000 connectivity DC showing >99.5% yield (~230-dies)—a significant improvement from pre-process optimization.

Die placement accuracy

Two bonding process cornerstones include bond force control and bond front propagation, of which the latter can be controlled through several options—with die shaping being preferred. The die shaping is responsible for creating a controlled bond front, ensuring no void entrapment, and avoiding ablation generated from the high-speed die bond to substrate wafer. Bond force, in turn, can impact initial bond strength from dielectric fusion as well as damage to the die if force is not controlled or not optimized.

Our approach to die shaping and bond front propagation is to have a single point of initial contact between die and substrate wafer, which is at the center of the die. This approach ensures two things: first, the initial contact causes instant bonding through Van der Waals's forces, thereby locking the die laterally and rotationally and minimizing placement accuracy loss from possible mechanical influences. Second, this allows the air between die and substrate wafer to be expelled symmetrically outwards as the die is flattened, thereby ensuring equal conditions on all sides of the die as well as minimizing risks of void entrapment. **Figure 10** shows the shape of the same die at different values of the variable-controlled factor for a 7x7mm die at thicknesses of 50µm and 100µm. The inner orange circle delineates that the die is at its highest warpage level taking on a convex shape. The graph shows that for the thinner 50µm die, the change in shape occurs at a much lower value for the controlled variable factor

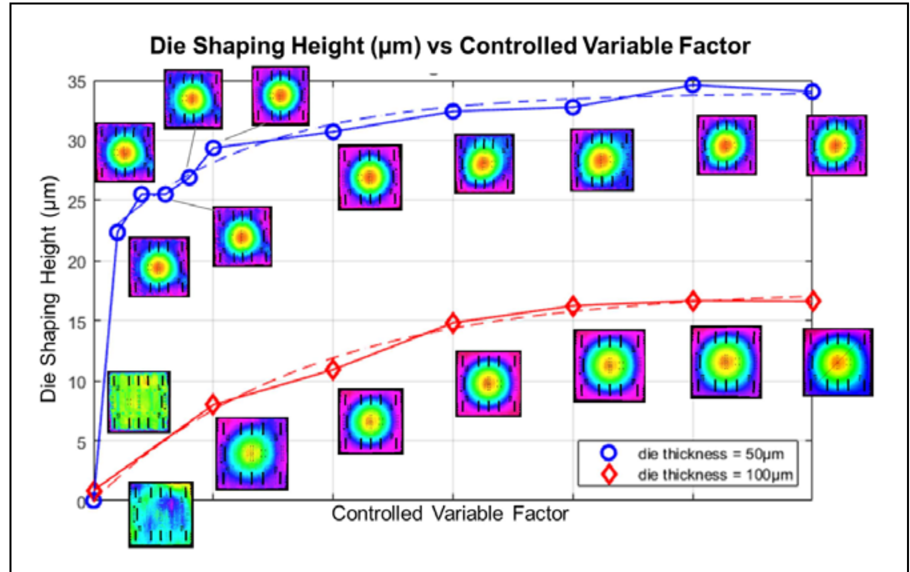

Figure 10: Die shaping height of die in µm vs. variation in the controllable factor for a 50µm (blue) and 100µm (red) thick die.

and that the maximum height is also higher. For the 100µm example, the die shows no deformation for the first four values of the controlled-variable factor. The maximum height is lower than the 50µm thick die, but both exhibit a similar behavior whereby the maximum die shape height flattens out. At all stages following the initial conditions however, the first point of contact is always in the center of the die.

Two scenarios were explored to estimate bonding precision. The first scenario is bonding on a substrate wafer coated with a temporary bonding material (TBM) layer. The second scenario consists of direct, or fusion, bonding. The first scenario uses a process that does not rely on plasma activation because the bonding mechanism is not through instantaneous fusion by way of Van der Waal's forces, but through the temporary bonding material adhesive. However, this process is reliant on the TBM's properties of bonding reaction times, elasticity and viscosity among others, all of which have an impact on final accuracy. The process was carried out with ~7x7mm dies analyzed using infrared (IR) microscopy. The results are shown in **Figure 11** and

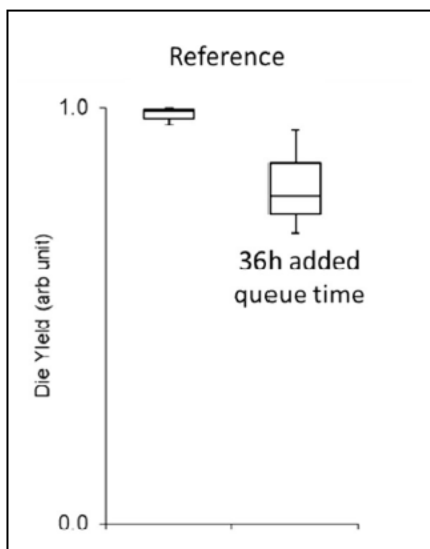

Figure 9: Plot showing the effect of added queue time on bonding yield.

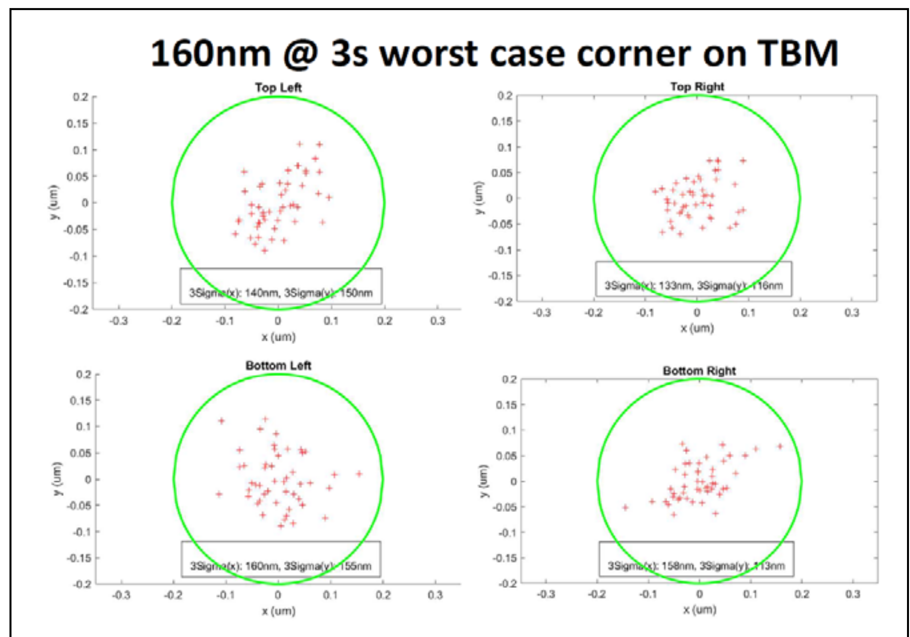

Figure 11: IR overlay for die placement on a wafer with a TBM layer.

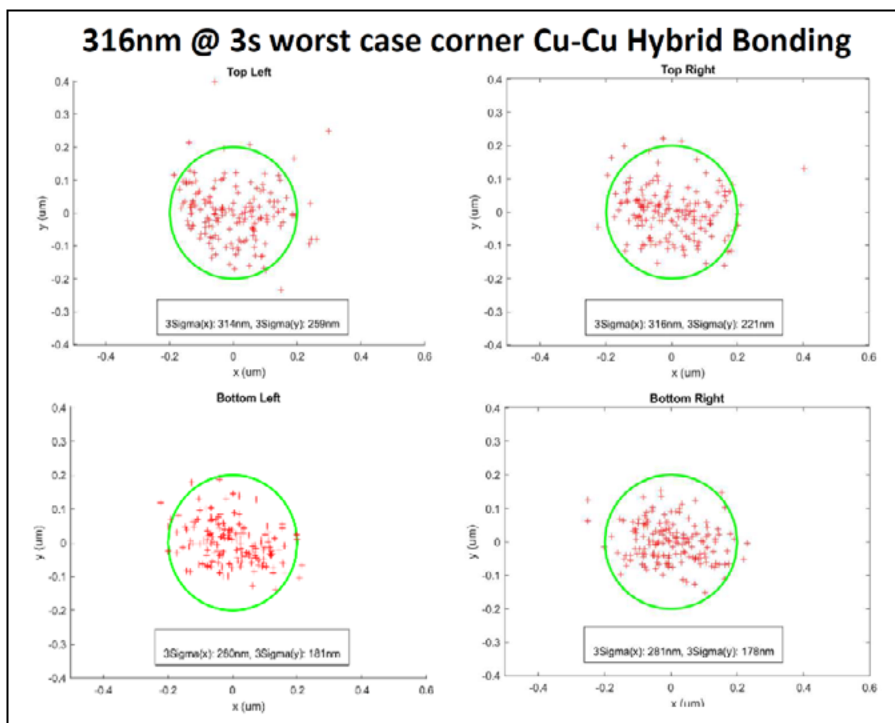

Figure 12: IR overlay for die placement on a wafer with direct bonding including a copper pad.

indicate that actual bond placement accuracy is an impressive 160nm @ ±3s for worst corner, which is currently one of the best die-to-wafer (D2W) accuracies. The green circle represents a ±200nm circle.

For the second scenario, the wafers were subjected to wet cleaning and plasma, as delineated in **Figure 1**. The dies in question were ~6x6mm. **Figure 12** shows placement accuracy results of 316nm @ ±3s for worst corner. The main factor for the gap in accuracy is that direct bonding is more prone to impact from customer material than any other bonding mechanism such as mentioned in the first part of this article due to its complexity and stringent requirements. Notwithstanding, 316nm @ ±3s for worst corner is still a very good result for a lab test vehicle and further trials with optimizations are planned in the future. The data shown in **Figure 12** was collected with an inline metrology system with feedback control capability.

Summary

A working process flow for D2W HB has been presented. Positive outcomes of an HVM-capable process heavily depend on the co-optimization of many pieces of a complex technical jigsaw. The bonding dielectric needs to be controlled in terms of surface roughness, and needs to be properly activated with plasma. Such plasma should not lead to damage to the dielectric, nor to the metal pads, which, in turn need to be controlled not just in terms of dishing, but also with regard to unwanted protrusions from the Ta barrier. The importance of cleanliness was clearly stated and demonstrated via studies showing void formations arising from particle entrapment. The bonding process itself was accomplished with advanced dynamic die-shaping capabilities, state of the art alignment (162nm @ 3σ), and using inline control capability. Finally, control of the queue time along the whole process is critical to guarantee optimal yield.

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References

1. W. L. I. C. C. a. C. H. Chiu, "Low-temperature wafer-to-wafer hybrid bonding by nanocrystalline copper," IEEE 72nd Elec. Comp. and Tech. Conf. (ECTC), 2022.
2. R. Agarwal, et al., "3D packaging for heterogeneous integration," 72nd ECTC, 2022.
3. S. Sitaraman, et al., "A holistic development framework for hybrid bonding," 72nd ECTC 2022.
4. V. Chidambaram, et al., "Dielectric materials characterization for hybrid bonding," IEEE 71st ECTC, San Diego, CA, USA, 2021.
5. "https://www.azom.com/properties.aspx?ArticleID=1114," [Online].
6. S. Son, et al., "Characteristics of plasma-activated dielectric film surfaces for direct wafer bonding," IEEE 70th ECTC, 2020.

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