Sub micron placement accuracy – the era for heterogeneous integration and optoelectronic assemblies

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Abstract

High-performance computing (HPC) architectures for artificial intelligence and data-centric workloads increasingly rely on heterogeneous integration to overcome limitations in device scaling, power efficiency, and system bandwidth. Advanced packaging technologies must therefore support aggressive interconnect pitch reduction, stringent alignment tolerances, and high interconnect integrity across logic chiplets, high-bandwidth memory, and emerging co-packaged optical interfaces. Conventional solder-based interconnect approaches face fundamental challenges at fine pitch.

This extended abstract addresses the challenges of advanced packaging. We will tackle hybrid bonding challenges and solutions as well as latest bonding results. Thermocompression bonding will also be addressed due to its increased importance for sub 20µm interconnect technologies, which are demanding not only higher accuracies but also fluxless bonding solutions. We will also tackle the requirements seen in the optoelectronic market, particularly for the transceiver side.

Keywords: submicron bonding, packaging, die to wafer (D2W) hybrid bonding, thermocompression bonding, TCB, fluxless TCB, optoelectronic assemblies.

I. INTRODUCTION

As illustrated in Figure 1, the ongoing AI era continues to drive innovation, creating an unrelenting demand for cutting-edge performance, greater power efficiency, and faster data transmission speeds. A key factor in meeting these demands is the adoption of smaller technology nodes for wafer fabrication, enabling a higher transistor density per unit area. However, this advancement necessitates an increased number of interconnects outside the die to enable die-to-die connectivity, presenting significant challenges, particularly when dealing with pitches below 20 µm. The other requirement to AI data centers is memory and their interlinking to 3d stacking. Hybrid bonding and thermocompression bonding (TCB) have merged as the interconnect technologies which can enable D2W bonding at sub 20µm pitches.

II. FUNDAMENTALS

One promising approach is the adoption of hybrid bonding (HB), which eliminates the reliance on traditional copper micro-bumps. This innovation facilitates the achievement of thinner vertical stacks, higher I/O density with tighter bond pad pitch, and reduced electrical and thermal resistance [1]. Hybrid bonding does not utilise any adhesives or intermediate material for die bonding, as depicted in Figure 2. The bonding is initiated by activating dielectric layers by plasma to create the dangling bonds and terminate the surfaces of the component dies and the substrate wafer with hydroxyl groups (-OH) by hydration, which are then bonded together at room temperature [2].

Hybrid bonding requires exceptionally clean and smooth surfaces because particles can create voids much larger than their own size, leading to interconnection failures [3]. Consequently, minimizing particle contamination from mechanical dicing is essential to enhance C2W hybrid bonding yield and facilitate broader market adoption.

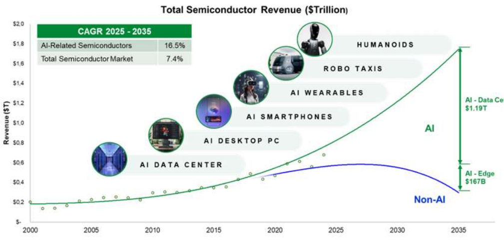
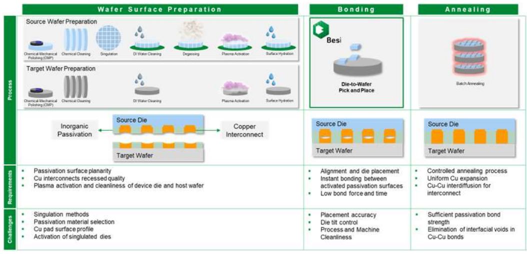


Figure 1. Megatrends over the years.

Thermo-compression bonding (TCB) employs copper pillars topped with solder caps to precisely control the amount and shape of solder once melted, enabling higher interconnect density. While there are various TCB methods, the core technique involves locally reflowing the solder while mechanically holding the die and substrate in place. As the die is retained, cooling occurs to solidify the solder, securing the die to the substrate and forming both mechanical and electrical joints. Typically, the die is only released after the solder has partially or fully solidified. This method enhances precision by removing dependence on solder self-alignment and minimizes warpage by maintaining flatness between the die and substrate throughout bonding. Additionally, TCB allows for active control of the bondline thickness (BLT), ensuring uniform solder interconnects and simplifying subsequent processes such as underfilling.



	Wafer Surface Preparation	Bonding	Annealing
Requirements	• Passivation surface planarity • Cu interconnects recessed quality • Plasma activation and cleanliness of device die and host wafer	• Alignment and die placement • Instant bonding between activated passivation surfaces • Low bond force and time	• Controlled annealing process • Uniform Cu expansion • Cu-Cu interdiffusion for interconnect
Challenges	• Singulation methods • Passivation material selection • Cu pad surface profile • Activation of singlulated dies	• Placement accuracy • Die tilt control • Process and Machine Cleanliness	• Sufficient passivation bond strength • Elimination of interfacial voids in Cu-Cu bonds

Figure 2. Hybrid Bonding Process Flow, Requirements and Challenges.

The TCB process requires a fluxing agent, applied either as a liquid or film. Unlike mass reflow flip-chip bonding, the flux in TCB does not need high tackiness to prevent die movement, since the die is mechanically fixed. Instead, its main role is to chemically reduce surface oxides during a controlled heating cycle, producing a clean, oxide-free, and solder-wettable metal surface essential for strong metallurgical bonds. The flux also aids in oxide reduction and enhances heat transfer throughout the bonding process [4].

Today’s applications demand dies with pitches below 20µm, presenting significant challenges for existing TCB solutions. To address these challenges, new methods known as fluxless TCB are being developed specifically for fine-pitch applications. As the name suggests, fluxless TCB eliminates the use of flux in any form - liquid, paste, or film. In this approach, the die featuring copper pillars and solder caps is bonded directly to the substrate without any intermediate medium. Three main flows are depicted in Figure 3.

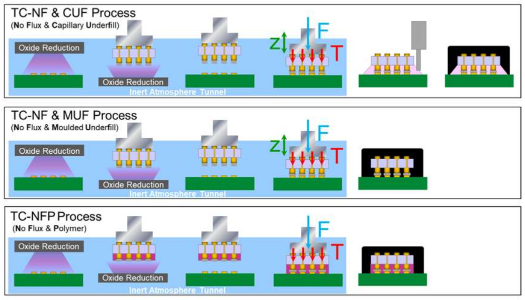


Figure 3. Fluxless TCB Scenarios

A critical aspect of fluxless TCB is the effective removal of oxidation prior to bonding, since oxides hinder solder wettability and prevent the formation of a strong metallurgical bond with the base materials. Additionally, the process must actively inhibit the formation of new oxides as temperatures rise during bonding, ensuring a clean metal surface throughout the TCB process.

With copper reaching its limit in terms of transfer speeds and energy usage, optoelectronic methods of data transmission are infiltrating the market to provide effective solutions. For such applications, especially on transceiver side, a myriad of die attach applications are needed, from UV adhesive attach with insitu curing, to die attach film (DAF) attach and even eutectic bonding.

III. RESULTS

Results for hybrid bonds done with IMEC material show

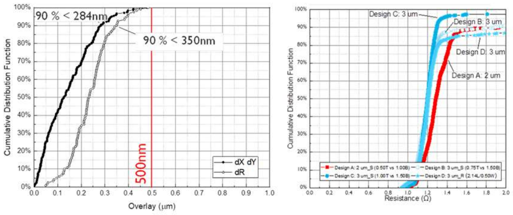


Figure 4. Accuracy and resistance results for hybrid bonds.

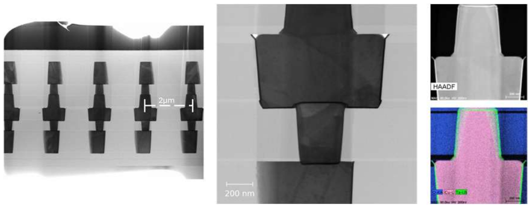


Figure 5. cross section of hybrid bonding at 2µm pitch.

For TCB a test vehicle comprising copper pillars with solder caps with 20µm, 10µm, 7µm and 5µm pitches was used, designed and fabricated by IMEC. Figure 6 (top) shows SEM images of the reflowed solder capped Cu pillars after insitu oxide reduction (inside TCB bonder) within an inert atmosphere tunnel with oxygen content less than 75ppm. The almost perfect spherical shapes show that oxide reduction was effective, otherwise the solder shape will not be smooth, as seen in Figure 6 (bottom). Results also show that at a fast 20mm/s process speed for oxide reduction at die level provided very good results in terms of electrical yield. The 5µm pitch showed low yield due to damaged bumps during wafer shipment. Results are in the process of being repeated.

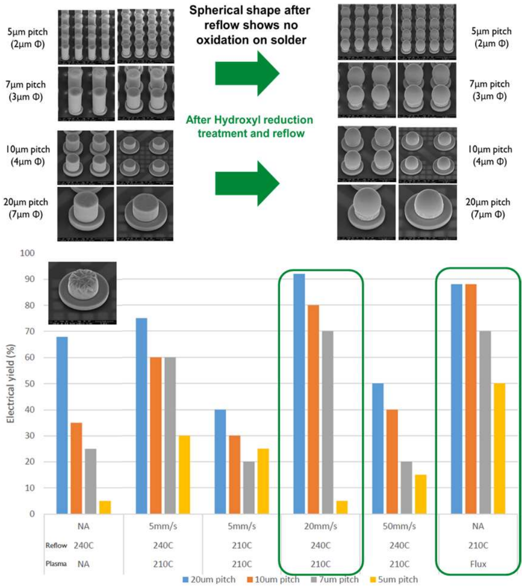


Figure 6. Cu pillar with solder caps showing spherical shapes after reflow (top); electrical yield results for several trials (bottom).

SEM images for 10µm and 5µm pitches can be seen in Figure 7 showing good points and placement accuracy. Resistance measurement was also performed showing a narrow distribution due to efficient H2 cleaning. 5µm pitch showed lower performance due to solder bridging. This is attributed to the fact that the amount of solder on the 5µm pitch Cu pillars is much higher than usual in order to meet the same height as all other Cu pillars, including the much larger 20µm pitch.

Actual measurements on the oxide thickness were also performed in collaboration with Nova, using their microspot XPS equipment. Results will be shared as well.

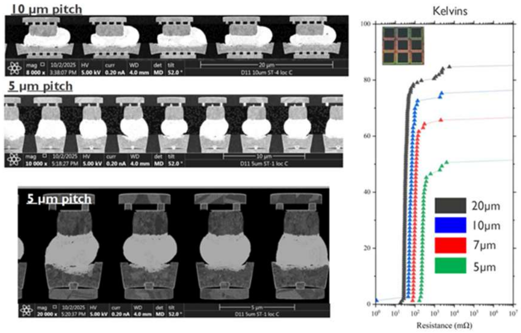


Figure 7. No flux bonding with oxide reduction SEM images (left); resistance measurements (right).

For optoelectronics looking into the multitude of components involved one notices the different interconnect methods as well as different placement accuracy requirements. Figure 8 gives an overview of a typical transceiver available in the market. This results in a myriad of different bonding equipment that has to be utilised to assemble such a module. Some results to cater for most of these applications in one sub micron accurate platform will also be discussed, which facilitates high volume manufacturing.

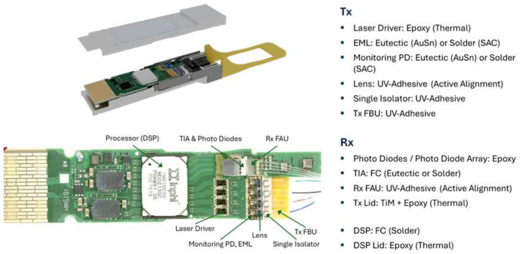


Figure 8. Typical transceiver breakdown and interconnect methods. Source: system plus & Besi.

IV. CONCLUSION

Advances in advanced packaging are reaching a limit whereby the complexity is demanding new forms of interconnect methods for sub micron accuracies, in the pursuit for a chiplet system to approach the performance of a monolithic chip. As the systems keep growing larger and transition to racks, particularly for AI datacentres, optical connections are required to keep up with dadta transfer rates and power consumption to transfer data. This abstract has highlighted the 2 main methods of D2W interconnect technologies with the most promise, mainly hybrid bonding and TCB. We also highlighted the complexity of such optoelectronic assemblies, focusing on transceivers. The market trend does not indicate a slow down in innovation and progress, and the current status is merely a stepping stone to something bigger which will manifest in the coming years.

V. ACKNOWLEDGEMENTS

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